Multiformat Video Encoder
Six, 11-Bit, 297 MHz DACs

ADV7342/ADV7343

FEATURES

- 74.25 MHz 20-/30-bit high definition input support
  - Compliant with SMPTE 274M (1080i), 296M (720p), and 240M (1035i)
- 6, 11-bit, 297 MHz video DACs
  - 16× (216 MHz) DAC oversampling for SD
  - 8× (216 MHz) DAC oversampling for ED
  - 4× (297 MHz) DAC oversampling for HD
  - 37 mA maximum DAC output current
- NTSC M, PAL B/D/G/H/I/M/N, PAL 60 support
- NTSC and PAL square pixel operation (24.54 MHz/29.5 MHz)
- Multiformat video input support
  - 4:2:2 YCrCb (SD, ED, and HD)
  - 4:4:4 YCrCb (ED and HD)
  - 4:4:4 RGB (SD, ED, and HD)
- Multiformat video output support
  - Composite (CVBS) and S-Video (Y/C)
  - Component YPrPb (SD, ED, and HD)
  - Component RGB (SD, ED, and HD)
- Macrovision® Rev 7.1.L1 (SD) and Rev 1.2 (ED) compliant
- Simultaneous SD and ED/HD operation
- EIA/CEA-861B compliance support
- Programmable features
  - Luma and chroma filter responses
  - Vertical blanking interval (VBI)
  - Subcarrier frequency (F_{SC}) and phase
  - Luma delay
- Copy generation management system (CGMS)
- Closed captioning and wide screen signaling (WSS)
- Integrated subcarrier locking to external video source
- Complete on-chip video timing generator
- On-chip test pattern generation
- On-board voltage reference (optional external input)
- Serial MPU interface with dual I²C® and SPI® compatibility
- 3.3 V analog operation
- 1.8 V digital operation
- 3.3 V I/O operation
- Temperature range: −40°C to +85°C

APPLICATIONS

- DVD recorders and players
- High definition Blu-ray DVD players
- HD-DVD players

FUNCTIONAL BLOCK DIAGRAM

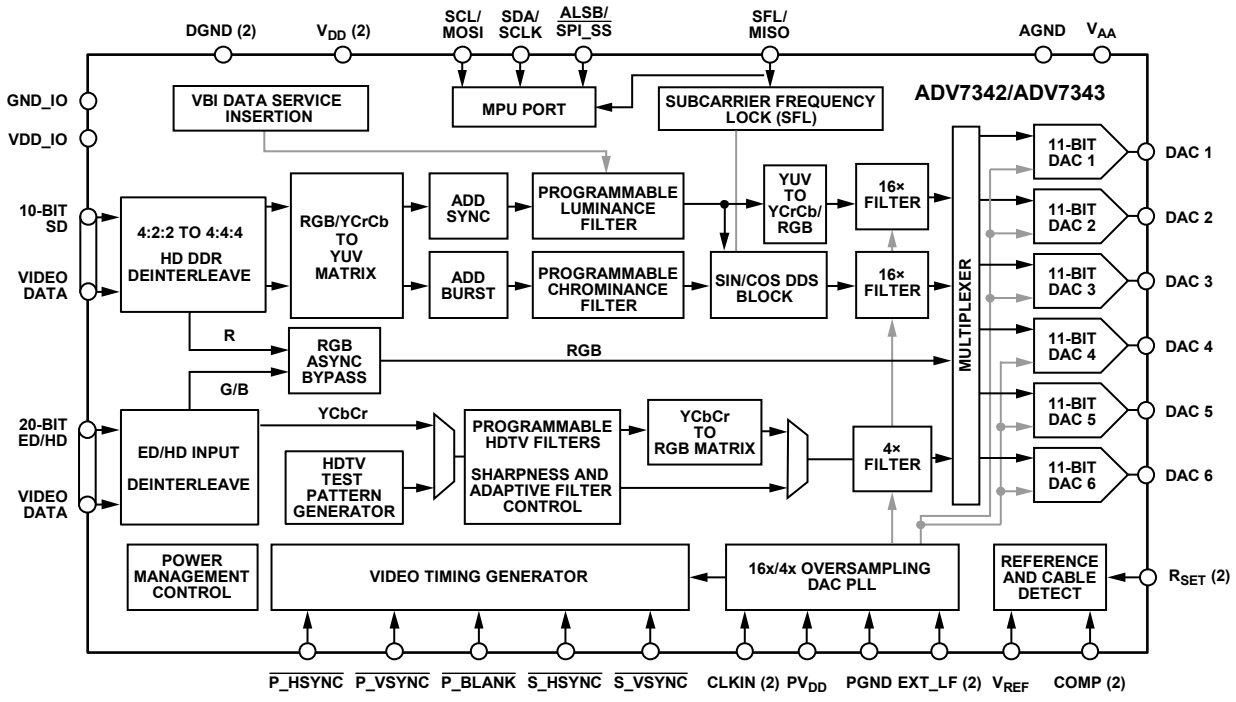

Figure 1.

Rev. 0

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REVISION HISTORY

10/06—Revision 0: Initial Version

DETAILED FEATURES

High definition (HD) programmable features
- **(720p/1080i/1035i)**
- **4× oversampling (297 MHz)**
- **Internal test pattern generator**
- **Fully programmable YCrCb to RGB matrix**
- **Gamma correction**
- **Programmable adaptive filter control**
- **Programmable sharpness filter control**
- **CGMS (720p/1080i) and CGMS Type B (720p/1080i)**
- **Undershoot limiter**
- **Dual data rate (DDR) input support**
- **EIA/CEA-861B compliance support**

Enhanced definition(ED) programmable features
- **(525p/625p)**
- **8× oversampling (216 MHz output)**
- **Internal test pattern generator**
  - **Color and black bar, hatch, flat field/frame**
- **Individual Y and PrPb output delay**
- **Gamma correction**
- **Programmable adaptive filter control**
- **Fully programmable YCrCb to RGB matrix**
- **Undershoot limiter**
- **Macrovision Rev 1.2 (525p/625p)**
- **CGMS (525p/625p) and CGMS Type B (525p)**
- **Dual data rate (DDR) input support**
- **EIA/CEA-861B compliance support**

Standard definition (SD) programmable features
- **16× oversampling (216 MHz)**
- **Internal test pattern generator**
  - **Color and black bar**
- **Controlled edge rates for start and end of active video**
- **Individual Y and PrPb output delay**
- **Undershoot limiter**
- **Gamma correction**
- **Digital noise reduction (DNR)**
- **Multiple chroma and luma filters**
- **Luma-SSAF™ filter with programmable gain/attenuation**
- **PrPb SSAF™**
- **Separate pedestal control on component and composite/S-Video output**
- **VCR FF/RW sync mode**
- **Macrovision Rev 7.1.L1**
- **Copy generation management system (CGMS)**
- **Wide screen signaling**
- **Closed captioning**
- **EIA/CEA-861B compliance support**

GENERAL DESCRIPTION

The ADV7342/ADV7343 are high speed, digital-to-analog video encoders in a 64-lead LQFP package. Six high speed, 3.3 V, 11-bit video DACs provide support for composite (CVBS), S-Video (Y/C), and component (YPrPb/RGB) analog outputs in either standard definition (SD), enhanced definition (ED), or high definition (HD) video formats.

The ADV7342/ADV7343 each have a 24-bit pixel input port that can be configured in a variety of ways. SD video formats are supported over a SDR interface and ED/HD video formats are supported over SDR and DDR interfaces. Pixel data can be supplied in either the YCrCb or RGB color spaces.

The parts also support embedded EAV/SAV timing codes, external video synchronization signals, and I²C and SPI communication protocols.

In addition, simultaneous SD and ED/HD input and output are supported. 216 MHz (SD and ED) and 297 MHz (HD) oversampling ensures that external output filtering is not required, while full-drive DACs ensure that external output buffering is not required.

Cable detection and DAC auto power-down features keep power consumption to a minimum.

Table 1 lists the video standards directly supported by the ADV7342/ADV7343.

Table 1. Standards Directly Supported by the ADV7342/ADV7343[1]

Resolution	I/P[2]	Frame Rate (Hz)	Clock Input (MHz)	Standard
720 × 240	P	59.94	27	
720 × 288	P	50	27	
720 × 480	I	29.97	27	ITU-R BT.601/656
720 × 576	I	25	27	ITU-R BT.601/656
720 × 480	I	29.97	24.54	NTSC Square Pixel
720 × 576	I	25	29.5	PAL Square Pixel
720 × 483	P	59.94	27	SMPTE 293M
720 × 483	P	59.94	27	BTA T-1004
720 × 483	P	59.94	27	ITU-R BT.1358
720 × 576	P	50	27	ITU-R BT.1358
720 × 483	P	59.94	27	ITU-R BT.1362
720 × 576	P	50	27	ITU-R BT.1362
1920 × 1035	I	30	74.25	SMPTE 240M
1920 × 1035	I	29.97	74.1758	SMPTE 240M
1280 × 720	P	60, 50, 30, 25, 24	74.25	SMPTE 296M
1280 × 720	P	23.97, 59.94, 29.97	74.1758	SMPTE 296M
1920 × 1080	I	30, 25	74.25	SMPTE 274M
1920 × 1080	I	29.97	74.1758	SMPTE 274M
1920 × 1080	P	30, 25, 24	74.25	SMPTE 274M
1920 × 1080	P	23.98, 29.97	74.1758	SMPTE 274M
1920 × 1080	P	24	74.25	ITU-R BT.709-5

[1] Other standards are supported in the ED/HD nonstandard timing mode.
[2] I = interlaced, P = progressive.

SPECIFICATIONS

POWER SUPPLY AND VOLTAGE SPECIFICATIONS

All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGES					
V_{DD}		1.71	1.8	1.89	V
V_{DD_IO}		2.97	3.3	3.63	V
PV_{DD}		1.71	1.8	1.89	V
V_{AA}		2.6	3.3	3.465	V
POWER SUPPLY REJECTION RATIO			0.002		%/%

VOLTAGE REFERENCE SPECIFICATIONS

All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
Internal Reference Range, V_{REF}		1.186	1.248	1.31	V
External Reference Range, V_{REF}		1.15	1.235	1.31	V
External V_{REF} Current[1]			±10		µA

[1] External current required to overdrive internal V_{REF}.

INPUT CLOCK SPECIFICATIONS

V_{DD} = 1.71 V to 1.89 V. PV_{DD} = 1.71 V to 1.89 V. V_{AA} = 2.6 V to 3.465 V. V_{DD_IO} = 2.97 V to 3.63 V.
All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 4.

Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CLKIN_A}	SD/ED		27		MHz
f_{CLKIN_A}	ED (at 54 MHz)		54		MHz
f_{CLKIN_A}	HD		74.25		MHz
f_{CLKIN_B}	ED		27		MHz
f_{CLKIN_B}	HD		74.25		MHz
CLKIN_A High Time, t_9		40			% of one clock cycle
CLKIN_A Low Time, t_{10}		40			% of one clock cycle
CLKIN_B High Time, t_9		40			% of one clock cycle
CLKIN_B Low Time, t_{10}		40			% of one clock cycle
CLKIN_A Peak-to-Peak Jitter Tolerance			2		±ns
CLKIN_B Peak-to-Peak Jitter Tolerance			2		±ns

[1] SD = standard definition, ED = enhanced definition (525p/625p), HD = high definition.

ANALOG OUTPUT SPECIFICATIONS

V_{DD} = 1.71 V to 1.89 V. PV_{DD} = 1.71 V to 1.89 V. V_{AA} = 2.6 V to 3.465 V. V_{DD_IO} = 2.97 V to 3.63 V. V_{REF} = 1.235 V (driven externally). All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
Full-Drive Output Current (Full-Scale)[1]	R_{SET} = 510 Ω, R_L = 37.5 Ω	33	34.6	37	mA
Low Drive Output Current (Full-Scale)[2]	R_{SET} = 4.12 kΩ, R_L = 300 Ω	4.1	4.3	4.5	mA
DAC-to-DAC Matching	DAC 1 to DAC 6		1.0		%
Output Compliance, V_{OC}		0		1.4	V
Output Capacitance, C_{OUT}	DAC 1, DAC 2, DAC 3		10		pF
	DAC 4, DAC 5, DAC 6		6		pF
Analog Output Delay[3]	DAC 1, DAC 2, DAC 3		8		ns
	DAC 4, DAC 5, DAC 6		6		ns
DAC Analog Output Skew	DAC 1, DAC 2, DAC 3		2		ns
	DAC 4, DAC 5, DAC 6		1		ns

[1] Applicable to full-drive capable DACs only, that is, DAC 1, DAC 2, DAC 3.
[2] Applicable to all DACs.
[3] Output delay measured from the 50% point of the rising edge of the input clock to the 50% point of the DAC output full-scale transition.

DIGITAL INPUT/OUTPUT SPECIFICATIONS

V_{DD} = 1.71 V to 1.89 V. PV_{DD} = 1.71 V to 1.89 V. V_{AA} = 2.6 V to 3.465 V. V_{DD_IO} = 2.97 V to 3.63 V. All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 6.

Parameter	Conditions	Min	Typ	Max	Unit
Input High Voltage, V_{IH}		2.0			V
Input Low Voltage, V_{IL}				0.8	V
Input Leakage Current, I_{IN}	V_{IN} = V_{DD_IO}			±10	μA
Input Capacitance, C_{IN}			4		pF
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Leakage Current	V_{IN} = 0.4 V, 2.4 V			±1.0	μA
Three-State Output Capacitance			4		pF

DIGITAL TIMING SPECIFICATIONS

V_{DD} = 1.71 V to 1.89 V. PV_{DD} = 1.71 V to 1.89 V. V_{AA} = 2.6 V to 3.465 V. V_{DD_IO} = 2.97 V to 3.63 V.
All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 7.

Parameter	Conditions[1]	Min	Typ	Max	Unit
VIDEO DATA AND VIDEO CONTROL PORT[2, 3]					
Data Setup Time, t_{11}[4]	SD	2.1			ns
	ED/HD-SDR	2.3			ns
	ED/HD-DDR	2.3			ns
	ED (at 54 MHz)	1.7			ns
Data Hold Time, t_{12}[4]	SD	1.0			ns
	ED/HD-SDR	1.1			ns
	ED/HD-DDR	1.1			ns
	ED (at 54 MHz)	1.0			ns
Control Setup Time, t_{11}[4]	SD	2.1			ns
	ED/HD-SDR or ED/HD-DDR	2.3			ns
	ED (at 54 MHz)	1.7			ns
Control Hold Time, t_{12}[4]	SD	1.0			ns
	ED/HD-SDR or ED/HD-DDR	1.1			ns
	ED (at 54 MHz)	1.0			ns
Digital Output Access Time, t_{13}[4]	SD			12	ns
	ED/HD-SDR, ED/HD-DDR or ED (at 54 MHz)			10	ns
Digital Output Hold Time, t_{14}[4]	SD	4.0			ns
	ED/HD-SDR, ED/HD-DDR or ED (at 54 MHz)	3.5			ns
PIPELINE DELAY[5]					
SD[1]					
CVBS/YC Outputs (2×)	SD oversampling disabled		68		clock cycles
CVBS/YC Outputs (16×)	SD oversampling enabled		67		clock cycles
Component Outputs (2×)	SD oversampling disabled		78		clock cycles
Component Outputs (16×)	SD oversampling enabled		84		clock cycles
ED[1]					
Component Outputs (1×)	ED oversampling disabled		41		clock cycles
Component Outputs (8×)	ED oversampling enabled		46		clock cycles
HD[1]					
Component Outputs (1×)	HD oversampling disabled		40		clock cycles
Component Outputs (4×)	HD oversampling enabled		44		clock cycles

[1] SD = standard definition, ED = enhanced definition (525p/625p), HD = high definition, SDR = single data rate, DDR = dual data rate.
[2] Video data: C[7:0], Y[7:0], and S[7:0].
[3] Video control: P_HSYNC, P_VSYNC, P_BLANK, S_HSYNC, and S_VSYNC.
[4] Guaranteed by characterization.
[5] Guaranteed by design.

MPU PORT TIMING SPECIFICATIONS

V_{DD} = 1.71 V to 1.89 V. PV_{DD} = 1.71 V to 1.89 V. V_{AA} = 2.6 V to 3.465 V. V_{DD_IO} = 2.97 V to 3.63 V.
All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 8.

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT, I²C MODE[1]	See Figure 19				
SCL Frequency		0		400	kHz
SCL High Pulse Width, t_1		0.6			µs
SCL Low Pulse Width, t_2		1.3			µs
Hold Time (Start Condition), t_3		0.6			µs
Setup Time (Start Condition), t_4		0.6			µs
Data Setup Time, t_5		100			ns
SDA, SCL Rise Time, t_6				300	ns
SDA, SCL Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			µs
MPU PORT, SPI MODE[1]	See Figure 20				
SCLK Frequency		0		10	MHz
$\overline{SPI\_SS}$ to SCLK Setup Time, t_1		20			ns
SCLK High Pulse Width, t_2		50			ns
SCLK Low Pulse Width, t_3		50			ns
Data Access Time after SCLK Falling Edge, t_4				35	ns
Data Setup Time prior to SCLK Rising Edge, t_5		20			ns
Data Hold Time after SCLK Rising Edge, t_6		0			ns
$\overline{SPI\_SS}$ to SCLK Hold Time, t_7		0			ns
$\overline{SPI\_SS}$ to MISO High Impedance, t_8				40	ns

[1] Guaranteed by characterization.

POWER SPECIFICATIONS

V_{DD} = 1.8 V, PV_{DD} = 1.8 V, V_{AA} = 3.3 V, V_{DD_IO} = 3.3 V, T_A = +25°C.

Table 9.

Parameter	Conditions	Min	Typ	Max	Unit
NORMAL POWER MODE[1, 2]					
I_{DD}[3]	SD only (16× oversampling)		90		mA
	ED only (8× oversampling)[4]		65		mA
	HD only (4× oversampling)[4]		91		mA
	SD (16× oversampling) and ED (8× oversampling)		95		mA
	SD (16× oversampling) and HD (4× oversampling)		122		mA
I_{DD_IO}			1		mA
I_{AA}	3 DACs enabled (ED/HD only)		124		mA
	6 DACs enabled (SD only and simultaneous modes)		140		mA
I_{PLL}	SD only, ED only or HD only modes		5		mA
	Simultaneous modes		10		mA
SLEEP MODE					
I_{DD}			5		µA
I_{AA}			0.3		µA
I_{DD_IO}			0.2		µA
I_{PLL}			0.1		µA

[1] R_{SET1} = 510 Ω (DAC 1, DAC 2, and DAC 3 operating in full-drive mode). R_{SET2} = 4.12 kΩ (DAC 4, DAC 5, and DAC 6 operating in low drive mode).
[2] 75% color bar test pattern applied to pixel data pins.
[3] I_{DD} is the continuous current required to drive the digital core.
[4] Applicable to both single data rate (SDR) and dual data rate (DDR) input modes.

VIDEO PERFORMANCE SPECIFICATIONS

V_{DD} = 1.8 V, PV_{DD} = 1.8 V, V_{AA} = 3.3 V, V_{DD_IO} = 3.3 V, T_A = 25°C, V_{REF} driven externally.

Table 10.

Parameter	Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE					
Resolution			11		Bits
Integral Nonlinearity	R_{SET1} = 510 kΩ, R_{L1} = 37.5 Ω		0.4		LSBs
	R_{SET2} = 4.12 kΩ, R_{L2} = 300 Ω		0.5		LSBs
Differential Nonlinearity[1] +ve	R_{SET1} = 510 kΩ, R_{L1} = 37.5 Ω		0.15		LSBs
	R_{SET2} = 4.12 kΩ, R_{L2} = 300 Ω		0.5		LSBs
Differential Nonlinearity[1] –ve	R_{SET1} = 510 kΩ, R_{L1} = 37.5 Ω		0.25		LSBs
	R_{SET2} = 4.12 kΩ, R_{L2} = 300 Ω		0.2		LSBs
STANDARD DEFINTION (SD) MODE					
Luminance Nonlinearity			0.5		±%
Differential Gain	NTSC		0.5		%
Differential Phase	NTSC		0.6		Degrees
Signal-to-Noise Ratio (SNR)	Luma ramp		58		dB
	Flat field full bandwidth		75		dB
ENHANCED DEFINITION (ED) MODE					
Luma Bandwidth			12.5		MHz
Chroma Bandwidth			5.8		MHz
HIGH DEFINITION (HD) MODE					
Luma Bandwidth			30		MHz
Chroma Bandwidth			13.75		MHz

[1] Differential nonlinearity (DNL) measures the deviation of the actual DAC output voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value. For –ve DNL, the actual step value lies below the ideal step value.

TIMING DIAGRAMS

The following abbreviations are used in Figure 2 to Figure 13:

- t_9 = Clock high time
- t_{10} = Clock low time
- t_{11} = Data setup time
- t_{12} = Data hold time
- t_{13} = Control output access time
- t_{14} = Control output hold time

In addition, refer to Table 31 for the ADV7342/ADV7343 input configuration.

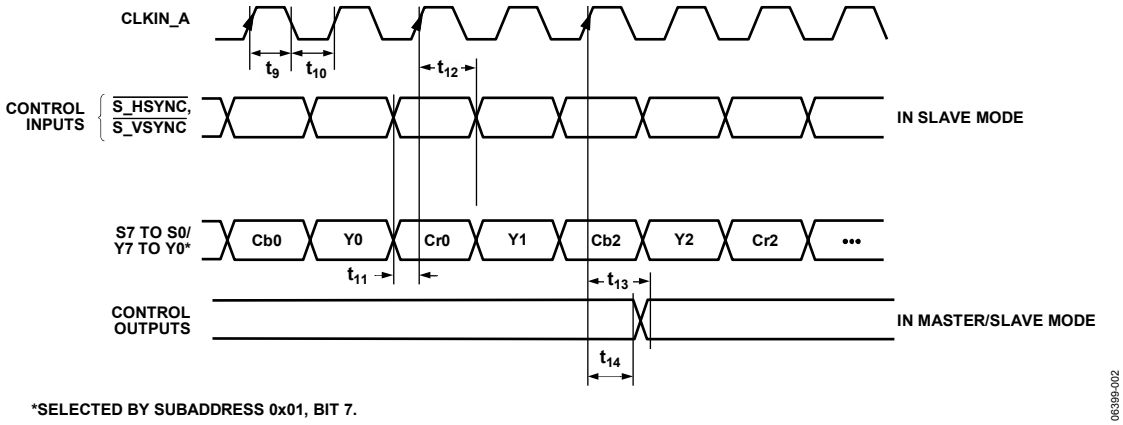


Figure 2. SD Only, 8-Bit, 4:2:2 YCrCb Pixel Input Mode (Input Mode 000)

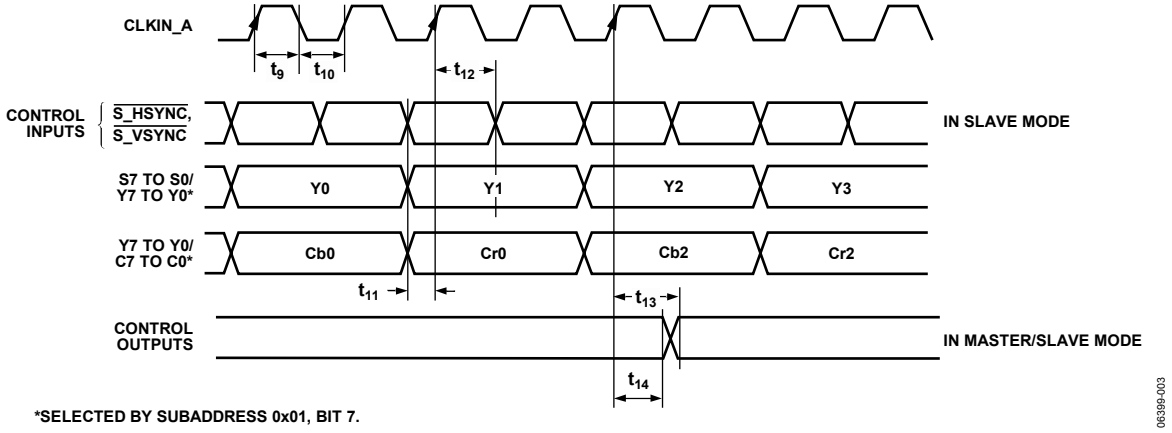


Figure 3. SD Only, 16-Bit, 4:2:2 YCrCb Pixel Input Mode (Input Mode 000)

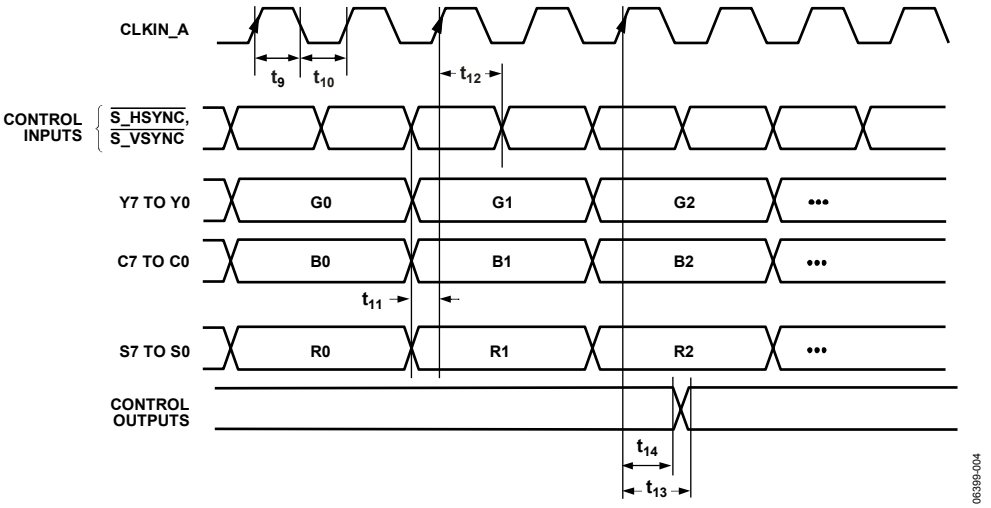


Figure 4. SD Only, 24-Bit, 4:4:4 RGB Pixel Input Mode (Input Mode 000)

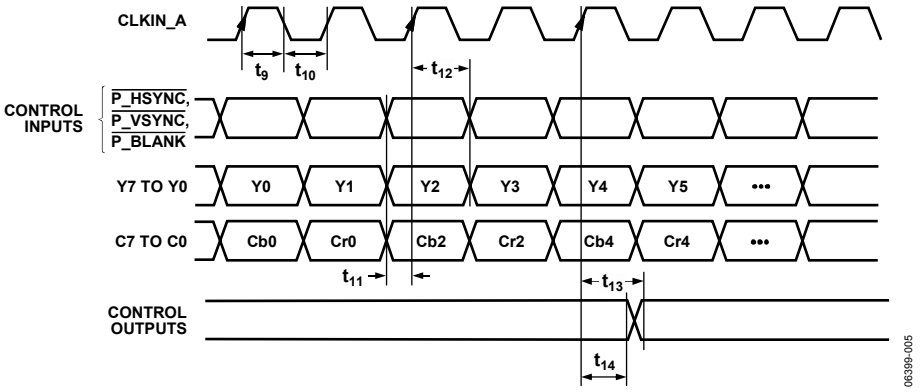


Figure 5. ED/HD-SDR Only, 16-Bit, 4:2:2 YCrCb Pixel Input Mode (Input Mode 001)

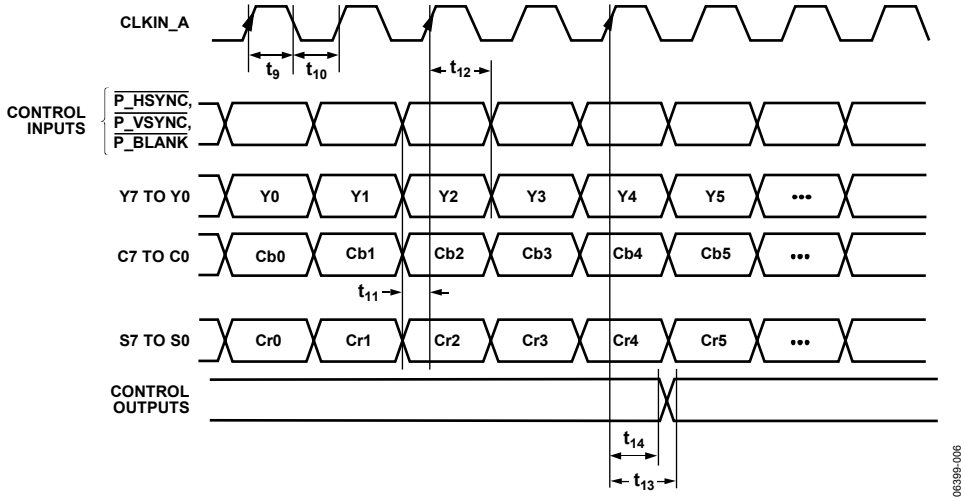


Figure 6. ED/HD-SDR Only, 24-Bit, 4:4:4 YCrCb Pixel Input Mode (Input Mode 001)

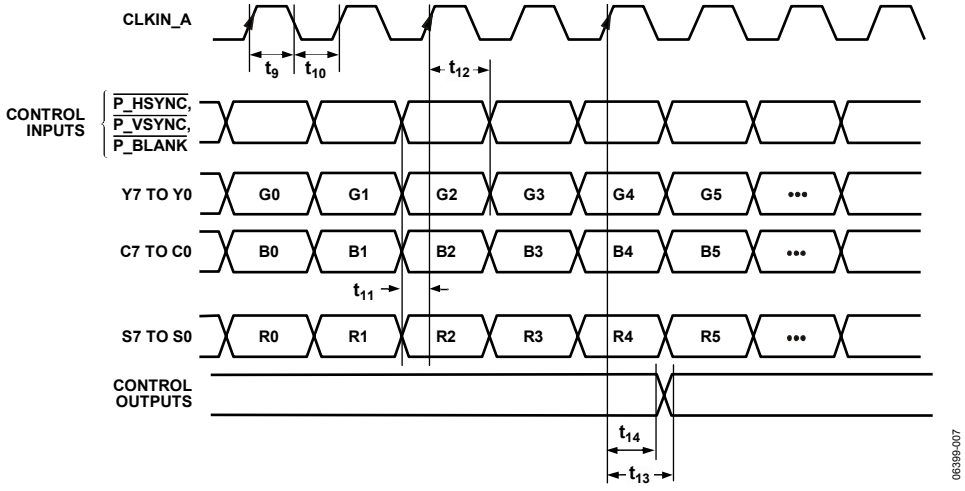


Figure 7. ED/HD-SDR Only, 24-Bit, 4:4:4 RGB Pixel Input Mode (Input Mode 001)

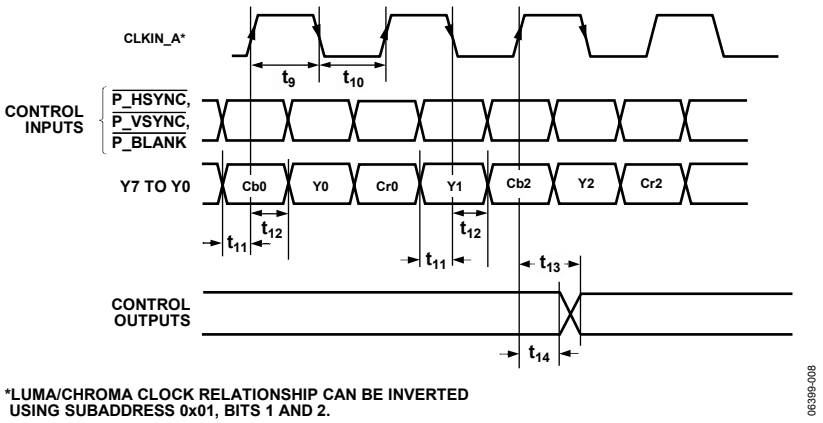


Figure 8. ED/HD-DDR Only, 8-Bit, 4:2:2 YCrCb ($\overline{HSYNC}$/$\overline{VSYNC}$) Pixel Input Mode (Input Mode 010)

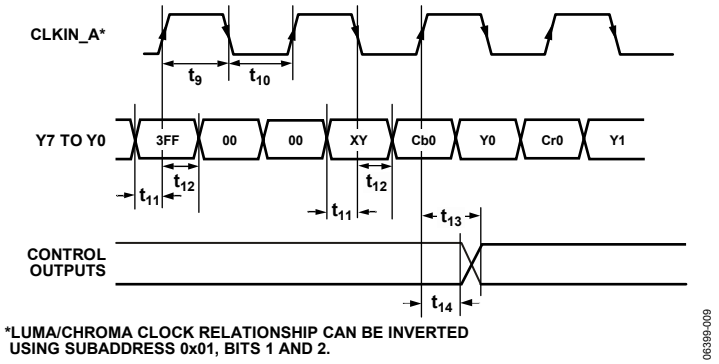


Figure 9. ED/HD-DDR Only, 8-Bit, 4:2:2 YCrCb (EAV/SAV) Pixel Input Mode (Input Mode 010)

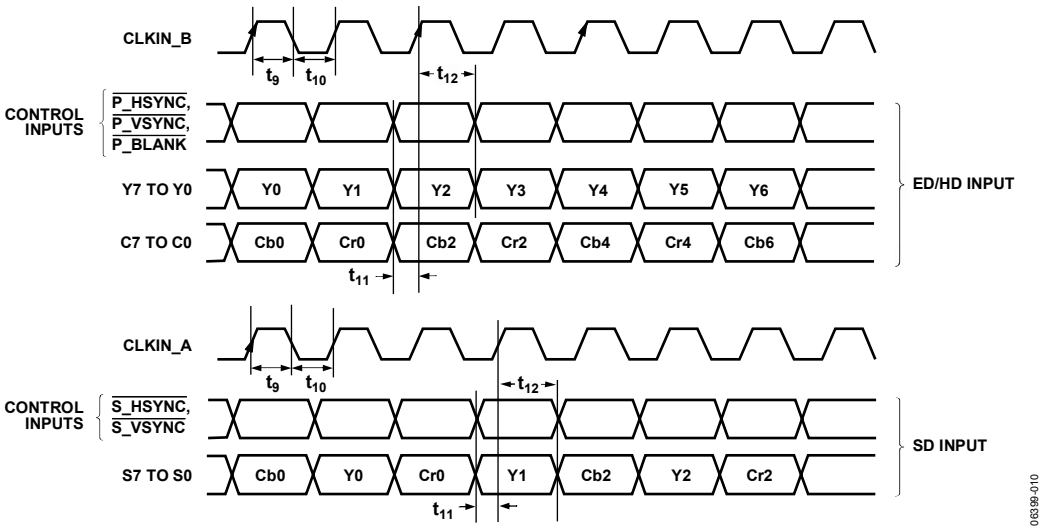


Figure 10. SD and ED/HD-SDR, 16-Bit, 4:2:2 ED/HD and 8-Bit, SD Pixel Input Mode (Input Mode 011)

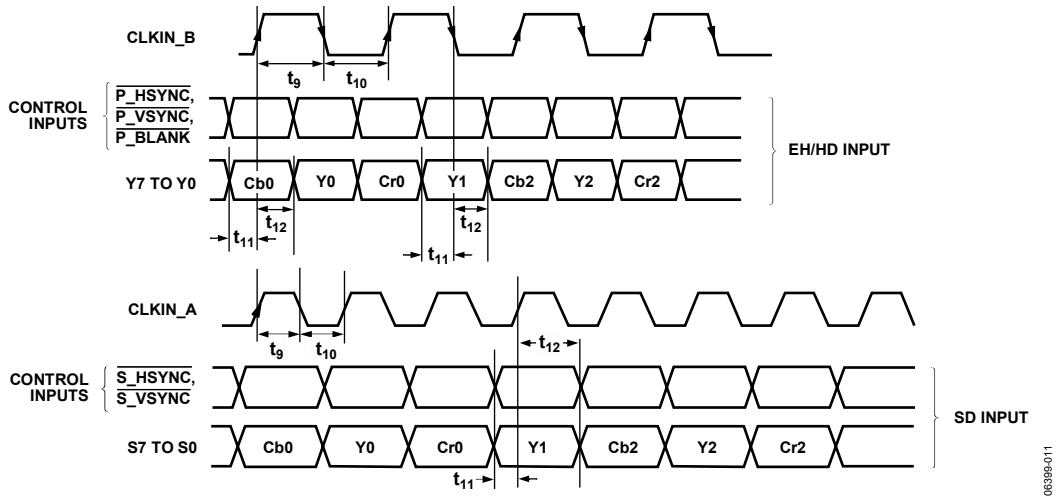


Figure 11. SD and ED/HD-DDR, 8-Bit, 4:2:2 ED/HD and 8-Bit, SD Pixel Input Mode (Input Mode 100)

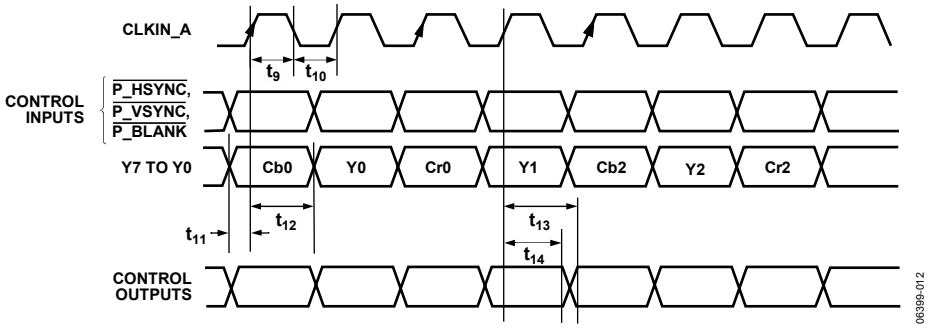


Figure 12. ED Only (at 54 MHz), 8-Bit, 4:2:2 YCrCb ($\overline{HSYNC}$/$\overline{VSYNC}$) Pixel Input Mode (Input Mode 111)

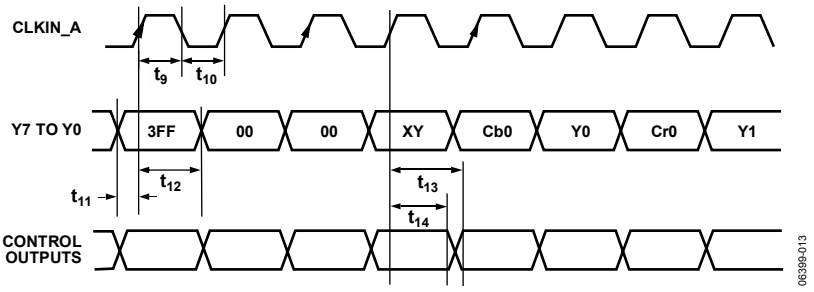
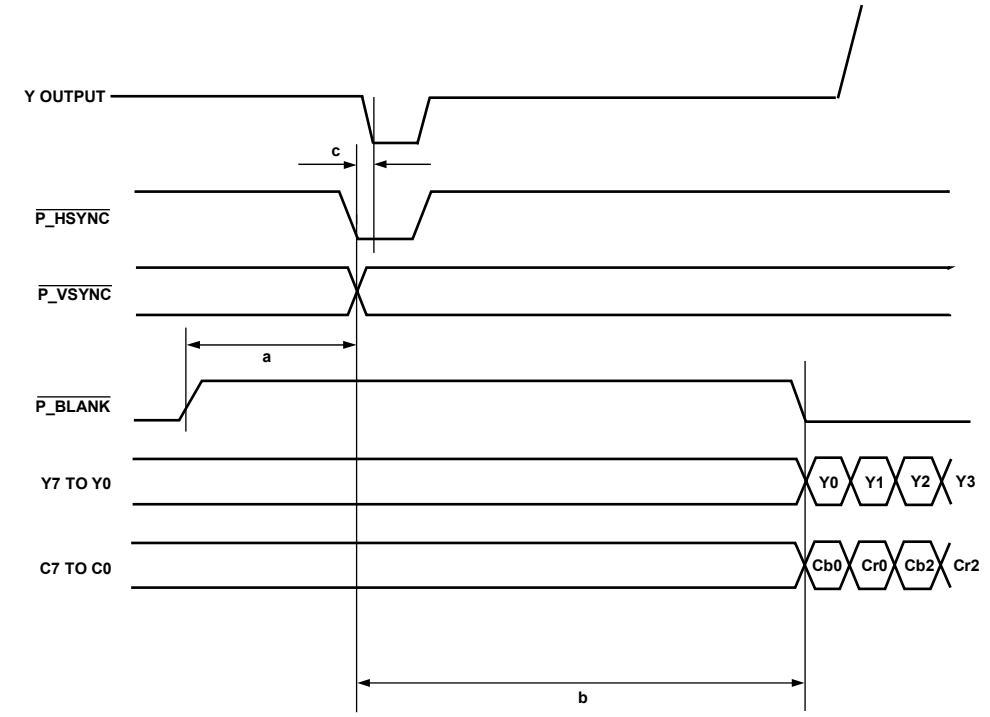


Figure 13. ED Only (at 54 MHz), 8-Bit, 4:2:2 YCrCb (EAV/SAV) Pixel Input Mode (Input Mode 111)



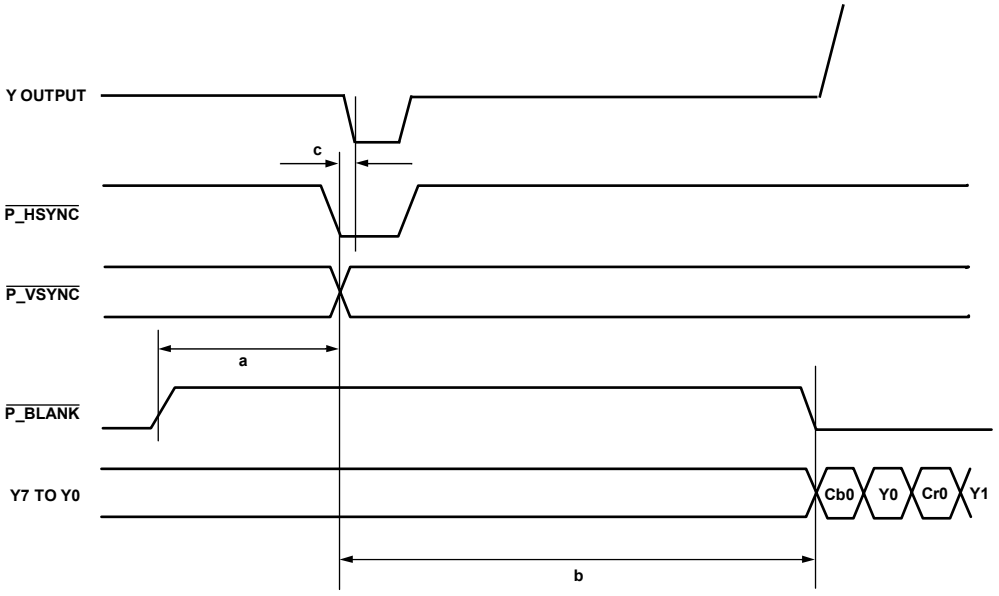
a AND b AS PER RELEVANT STANDARD.

c = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A SYNC FALLING EDGE ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06399-014

Figure 14. ED-SDR, 16-Bit, 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram



a = 32 CLOCK CYCLES FOR 525p
a = 24 CLOCK CYCLES FOR 625p
AS RECOMMENDED BY STANDARD

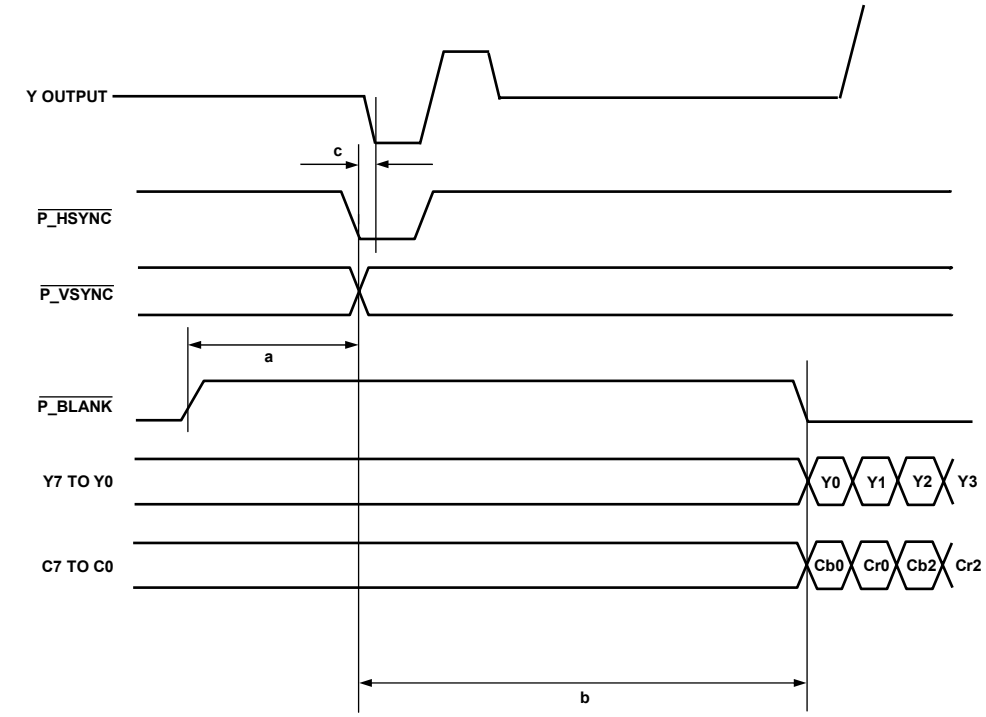
b(MIN) = 244 CLOCK CYCLES FOR 525p
b(MIN) = 264 CLOCK CYCLES FOR 625p

c = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A SYNC FALLING EDGE ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06399-015

Figure 15. ED-DDR, 8-Bit, 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram



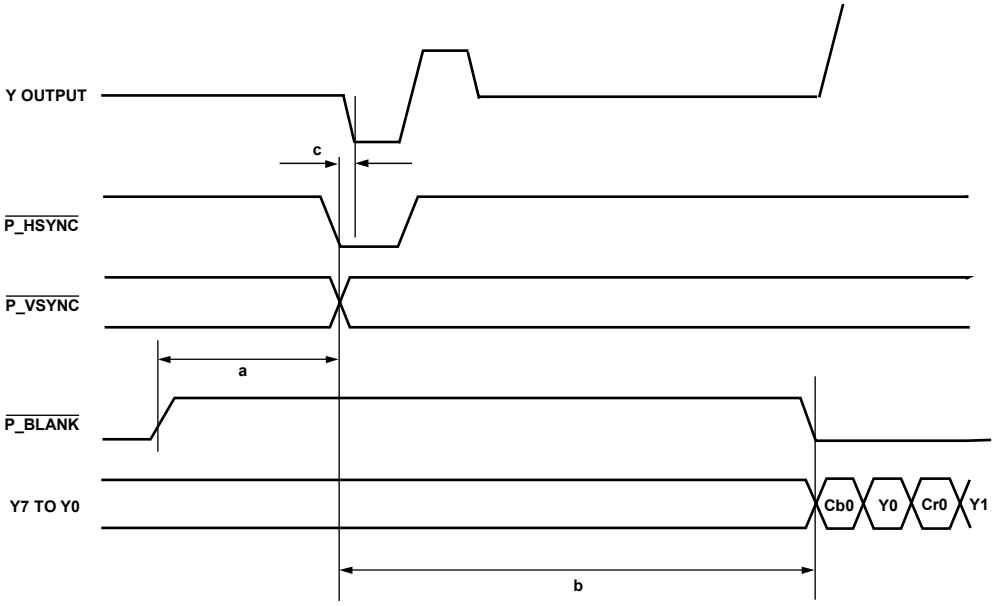
a AND b AS PER RELEVANT STANDARD.

c = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A FALLING EDGE OF TRI-LEVEL SYNC ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06399-016

Figure 16. HD-SDR, 16-Bit, 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram



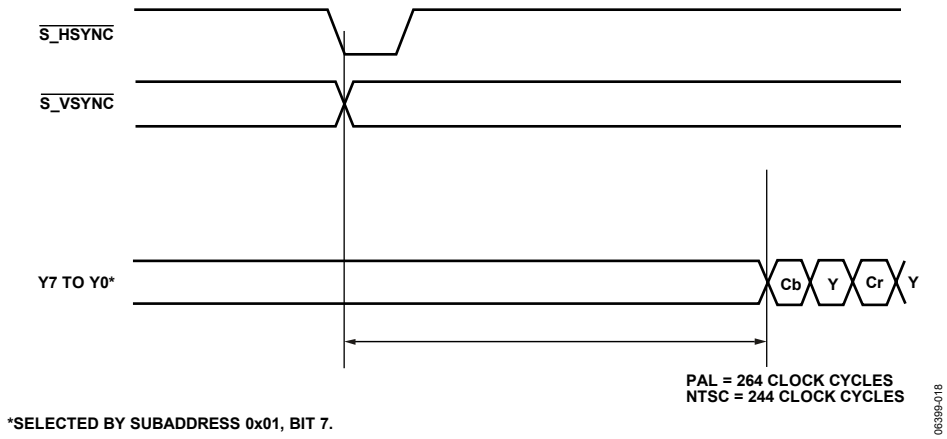
a AND b AS PER RELEVANT STANDARD.

c = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A FALLING EDGE OF TRI-LEVEL SYNC ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06399-017

Figure 17. HD-DDR, 8-Bit, 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram



*SELECTED BY SUBADDRESS 0x01, BIT 7.

Figure 18. SD Input Timing Diagram (Timing Mode 1)

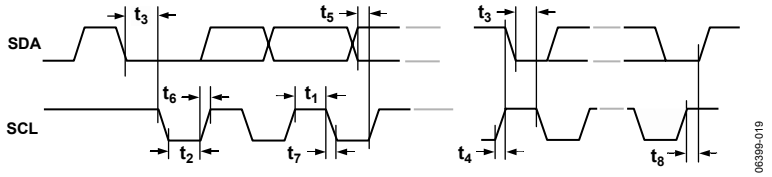


Figure 19. MPU Port Timing Diagram (I²C Mode)

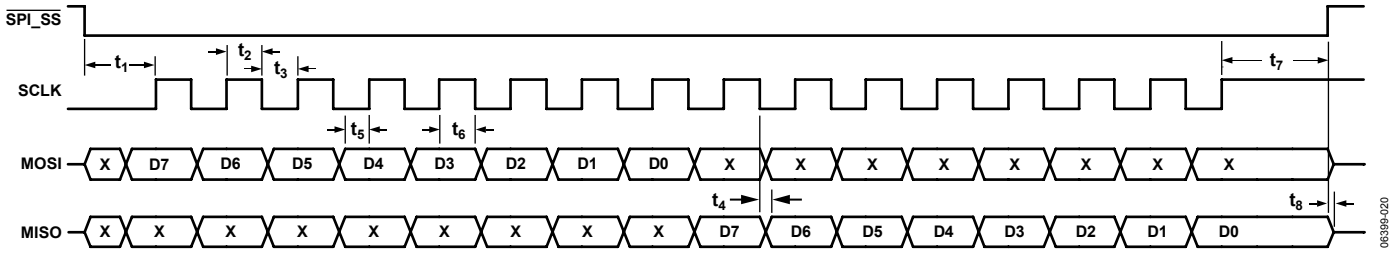


Figure 20. MPU Port Timing Diagram (SPI Mode)

ABSOLUTE MAXIMUM RATINGS

Table 11.

Parameter[1]	Rating
V_{AA} to AGND	−0.3 V to +3.9 V
V_{DD} to DGND	−0.3 V to +2.3 V
PV_{DD} to PGND	−0.3 V to +2.3 V
V_{DD_IO} to GND_IO	−0.3 V to +3.9 V
V_{AA} to V_{DD}	−0.3 V to +2.2 V
V_{DD} to PV_{DD}	−0.3 V to +0.3 V
V_{DD_IO} to V_{DD}	−0.3 V to +2.2 V
AGND to DGND	−0.3 V to +0.3 V
AGND to PGND	−0.3 V to +0.3 V
AGND to GND_IO	−0.3 V to +0.3 V
DGND to PGND	−0.3 V to +0.3 V
DGND to GND_IO	−0.3 V to +0.3 V
PGND to GND_IO	−0.3 V to +0.3 V
Digital Input Voltage to GND_IO	−0.3 V to V_{DD_IO} + 0.3 V
Analog Outputs to AGND	−0.3 V to V_{AA}
Storage Temperature Range (T_S)	−65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10 sec)	260°C

[1] Analog output short circuit to any power supply or common can be of an indefinite duration.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The ADV7342/ADV7343 are high performance integrated circuits with an ESD rating of <1 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 12. Thermal Resistance[1]

Package Type	θ_{JA}	θ_{JC}	Unit
64-Lead LQFP	47	11	°C/W

[1] Values are based on a JEDEC 4 layer test board.

The ADV7342/ADV7343 are Pb-free products. The lead finish is 100% pure Sn electroplate. The devices are RoHS compliant, suitable for Pb-free applications up to 255°C (±5°C) IR reflow (JEDEC STD-20).

They are backward-compatible with conventional SnPb soldering processes. The electroplated Sn coating can be soldered with Sn/Pb solder paste at conventional reflow temperatures of 220°C to 235°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

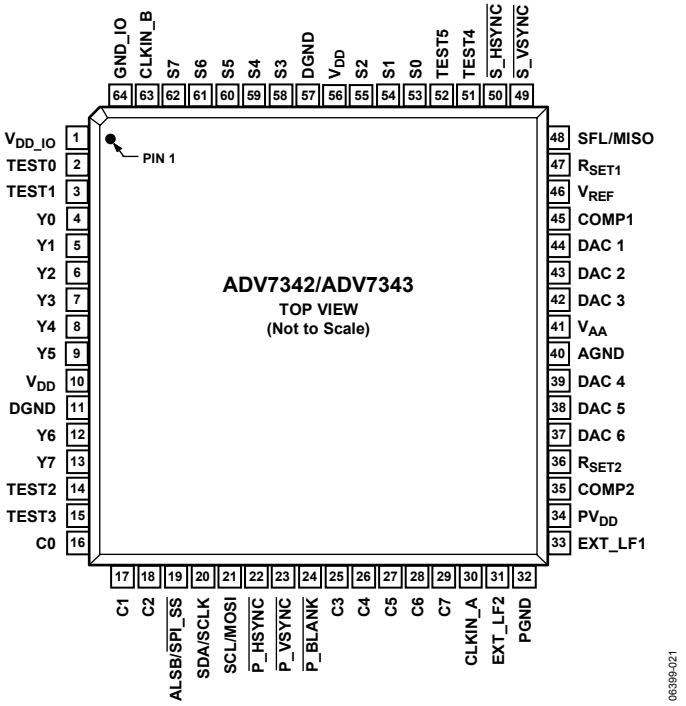


Figure 21. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output	Description
13, 12, 9 to 4	Y7 to Y0	I	8-Bit Pixel Port. Y0 is the LSB. Refer to Table 31 for input modes.
29 to 25, 18 to 16	C7 to C0	I	8-Bit Pixel Port. C0 is the LSB. Refer to Table 31 for input modes.
62 to 58, 55 to 53	S7 to S0	I	8-Bit Pixel Port. S0 is the LSB. Refer to Table 31 for input modes.
52, 51, 15, 14, 3, 2	TEST5 to TEST0	I	Unused. These pins should be connected to DGND.
30	CLKIN_A	I	Pixel Clock Input for HD Only (74.25 MHz), ED[1] Only (27 MHz or 54 MHz) or SD Only (27 MHz).
63	CLKIN_B	I	Pixel Clock Input for Dual Modes Only. Requires a 27 MHz reference clock for ED operation or a 74.25 MHz reference clock for HD operation.
50	$\overline{\text{S\_HSYNC}}$	I/O	SD Horizontal Synchronization Signal. This pin can also be configured to output an SD, ED, or HD horizontal synchronization signal. See the External Horizontal and Vertical Synchronization Control section.
49	$\overline{\text{S\_VSYNC}}$	I/O	SD Vertical Synchronization Signal. This pin can also be configured to output an SD, ED, or HD vertical synchronization signal. See the External Horizontal and Vertical Synchronization Control section.
22	$\overline{\text{P\_HSYNC}}$	I	ED/HD Horizontal Synchronization Signal. See the External Horizontal and Vertical Synchronization Control section.
23	$\overline{\text{P\_VSYNC}}$	I	ED/HD Vertical Synchronization Signal. See the External Horizontal and Vertical Synchronization Control section.
24	$\overline{\text{P\_BLANK}}$	I	ED/HD Blanking Signal. See the External Horizontal and Vertical Synchronization Control section.
48	SFL/MISO	I/O	Multifunctional Pin: Subcarrier Frequency Lock (SFL) Input/SPI Data Output. The SFL input is used to drive the color subcarrier DDS system, timing reset, or subcarrier reset.
47	R_{SET1}	I	This pin is used to control the amplitudes of the DAC 1, DAC 2, and DAC 3 outputs. For full-drive operation (for example, into a 37.5 Ω load), a 510 Ω resistor must be connected from R_{SET1} to AGND. For low drive operation (for example, into a 300 Ω load), a 4.12 kΩ resistor must be connected from R_{SET1} to AGND.

Pin No.	Mnemonic	Input/ Output	Description
36	R_{SET2}	I	This pin is used to control the amplitudes of the DAC 4, DAC 5, and DAC 6 outputs. A 4.12 kΩ resistor must be connected from R_{SET2} to AGND.
45, 35	COMP1, COMP2	O	Compensation Pins. Connect a 2.2 nF capacitor from both COMP pins to V_{AA}.
44, 43, 42	DAC 1, DAC 2, DAC 3	O	DAC Outputs. Full and low drive capable DACs.
39, 38, 37	DAC 4, DAC 5, DAC 6	O	DAC Outputs. Low drive only capable DACs.
21	SCL/MOSI	I	Multifunctional Pin: I²C Clock Input/SPI Data Input.
20	SDA/SCLK	I/O	Multifunctional Pin: I²C Data Input/Output. Also, SPI clock input.
19	ALSB/$\overline{\text{SPI\_SS}}$	I	Multifunctional Pin: This signal sets up the LSB[2] of the MPU I²C address. Also, SPI slave select.
46	V_{REF}		Optional External Voltage Reference Input for DACs or Voltage Reference Output.
41	V_{AA}	P	Analog Power Supply (3.3 V).
10, 56	V_{DD}	P	Digital Power Supply (1.8 V). For dual-supply configurations, V_{DD} can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering.
1	V_{DD_IO}	P	Input/Output Digital Power Supply (3.3 V).
34	PV_{DD}	P	PLL Power Supply (1.8 V). For dual-supply configurations, PV_{DD} can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering.
33	EXT_LF1	I	External Loop Filter for On-Chip PLL 1.
31	EXT_LF2	I	External Loop Filter for On-Chip PLL 2.
32	PGND	G	PLL Ground Pin.
40	AGND	G	Analog Ground Pin.
11, 57	DGND	G	Digital Ground Pin.
64	GND_IO	G	Input/Output Supply Ground Pin.

[1] ED = enhanced definition = 525p and 625p.
[2] LSB = least significant bit. In the ADV7342, setting the LSB to 0 sets the I²C address to 0xD4. Setting it to 1 sets the I²C address to 0xD6. In the ADV7343, setting the LSB to 0 sets the I²C address to 0x54. Setting it to 1 sets the I²C address to 0x56.

TYPICAL PERFORMANCE CHARACTERISTICS

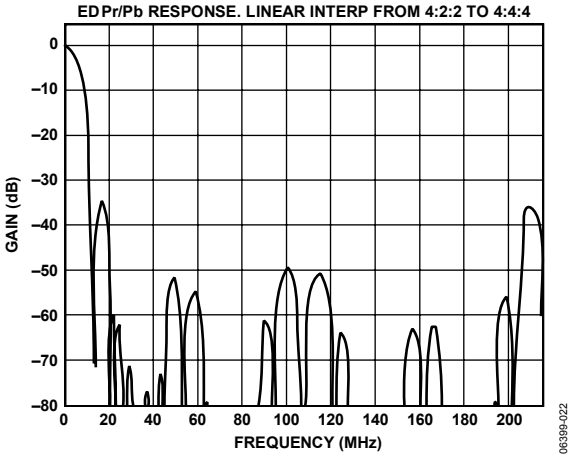


Figure 22. ED 8× Oversampling, PrPb Filter (Linear) Response

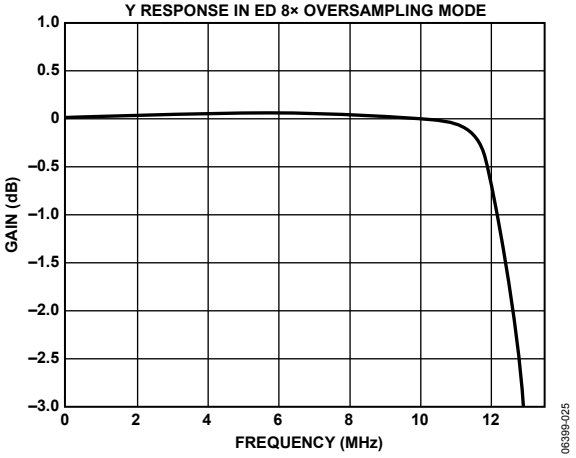


Figure 25. ED 8× Oversampling, Y Filter Response (Focus on Pass Band)

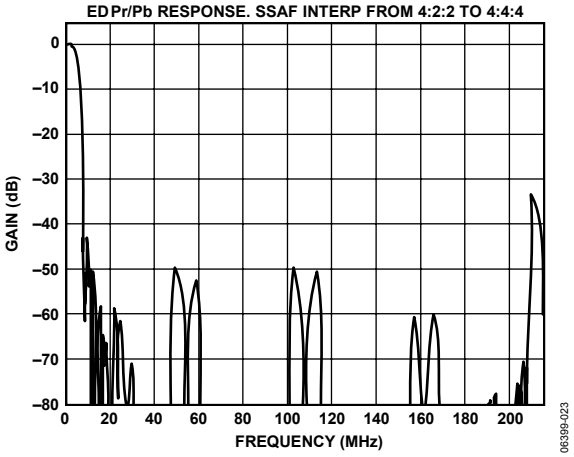


Figure 23. ED 8× Oversampling, PrPb Filter (SSAF) Response

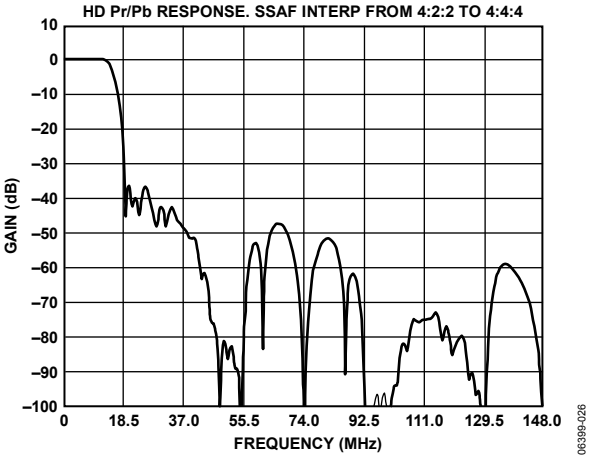


Figure 26. HD 4× Oversampling, PrPb (SSAF) Filter Response (4:2:2 Input)

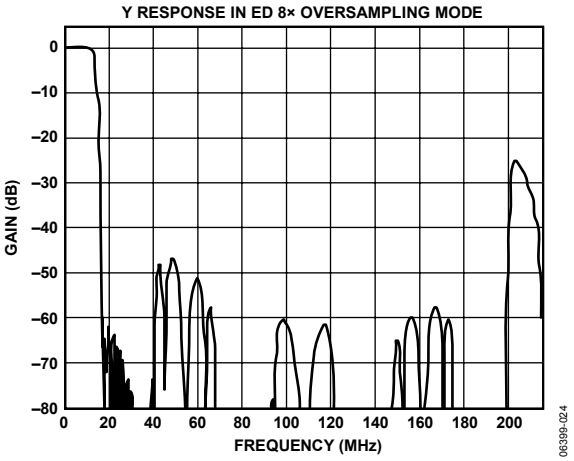


Figure 24. ED 8× Oversampling, Y Filter Response

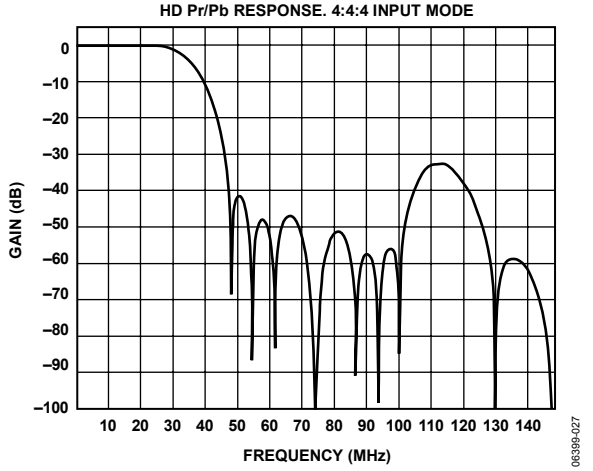


Figure 27. HD 4× Oversampling, PrPb (SSAF) Filter Response (4:4:4 Input)

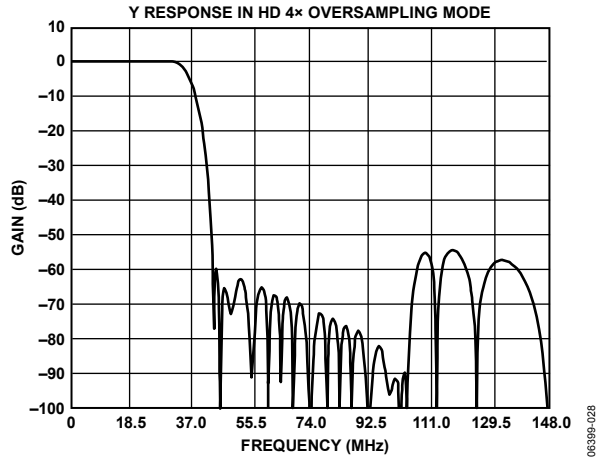


Figure 28. HD 4× Oversampling, Y Filter Response

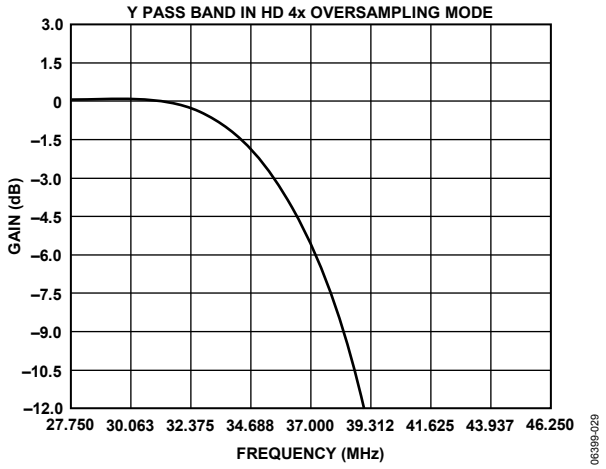


Figure 29. HD 4× Oversampling, Y Filter Response (Focus on Pass Band)

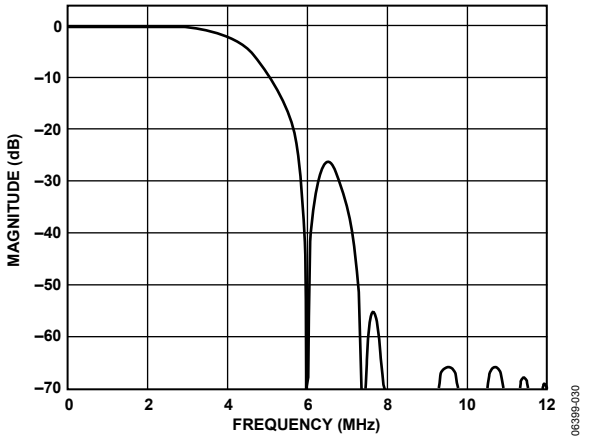


Figure 30. SD NTSC, Luma Low-Pass Filter Response

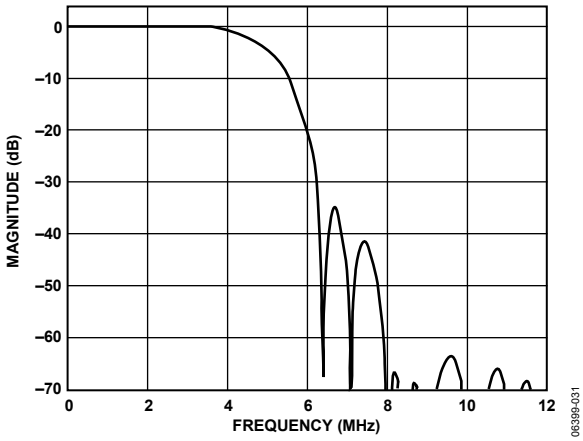


Figure 31. SD PAL, Luma Low-Pass Filter Response

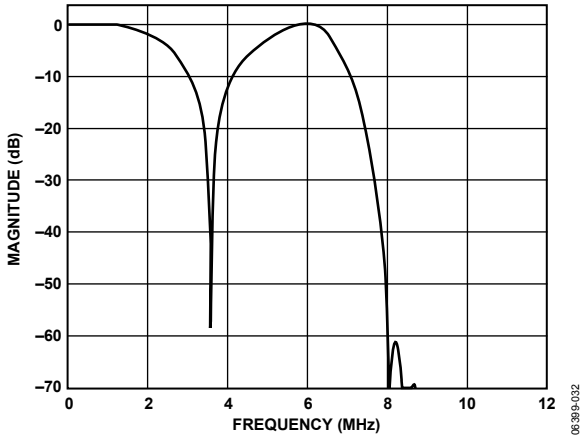


Figure 32. SD NTSC, Luma Notch Filter Response

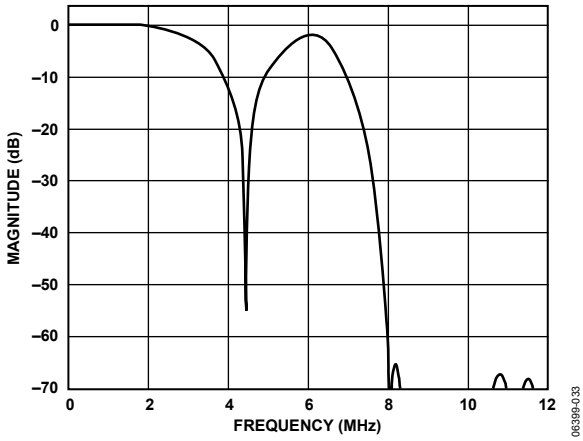


Figure 33. SD PAL, Luma Notch Filter Response

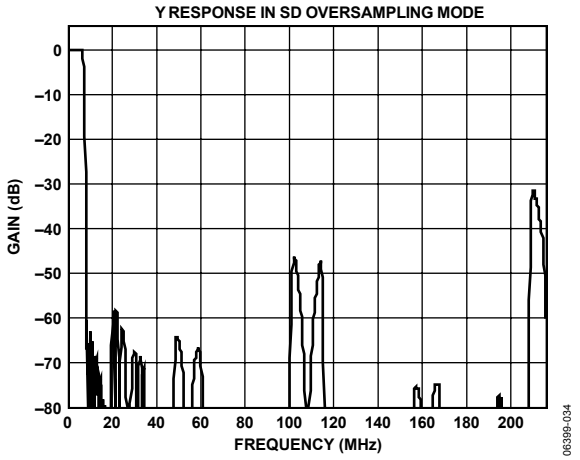


Figure 34. SD, 16× Oversampling, Y Filter Response

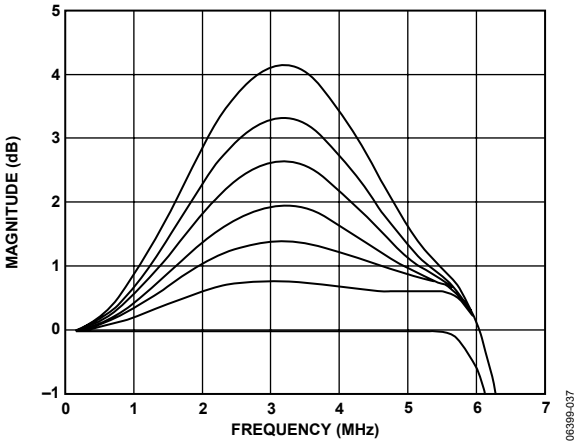


Figure 37. SD Luma SSAF Filter, Programmable Gain

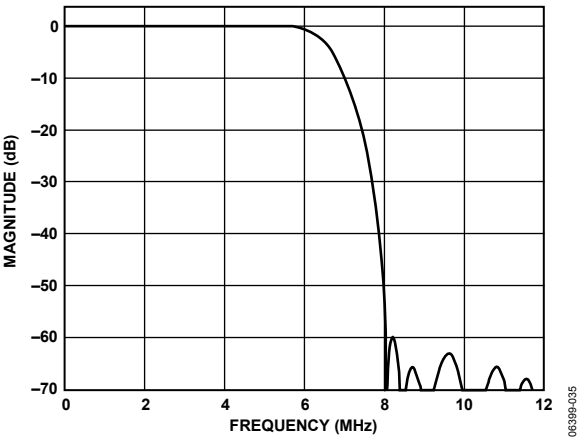


Figure 35. SD Luma SSAF Filter Response up to 12 MHz

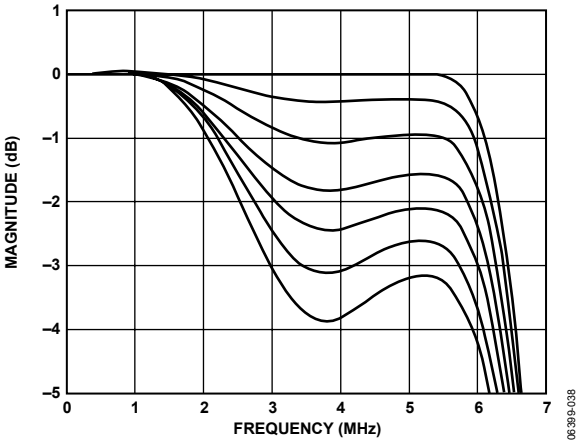


Figure 38. SD Luma SSAF Filter, Programmable Attenuation

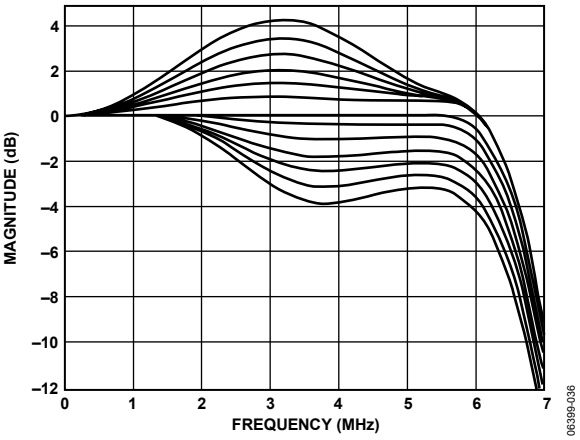


Figure 36. SD Luma SSAF Filter, Programmable Responses

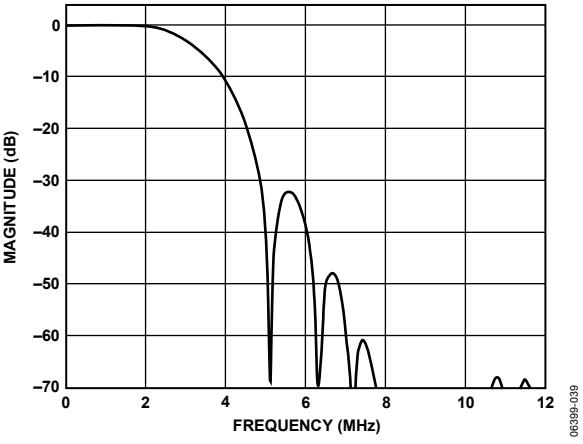


Figure 39. SD Luma CIF Low-Pass Filter Response

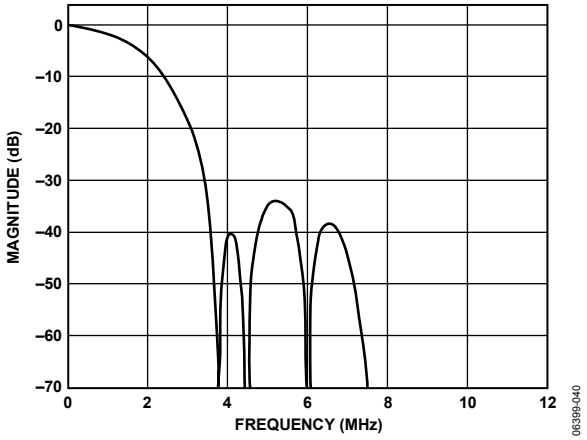


Figure 40. SD Luma QCIF Low-Pass Filter Response

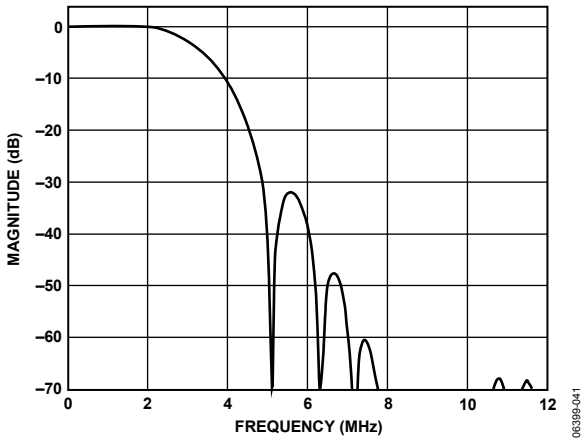


Figure 41. SD Chroma 3.0 MHz Low-Pass Filter Response

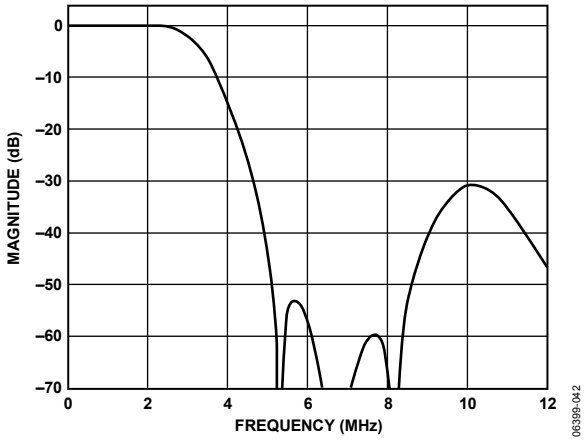


Figure 42. SD Chroma 2.0 MHz Low-Pass Filter Response

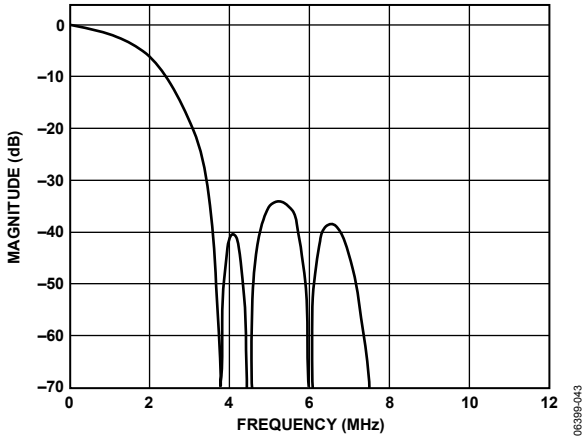


Figure 43. SD Chroma 1.3 MHz Low-Pass Filter Response

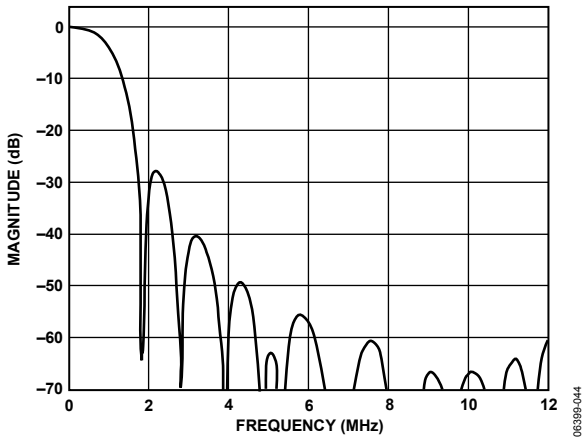


Figure 44. SD Chroma 1.0 MHz Low-Pass Filter Response

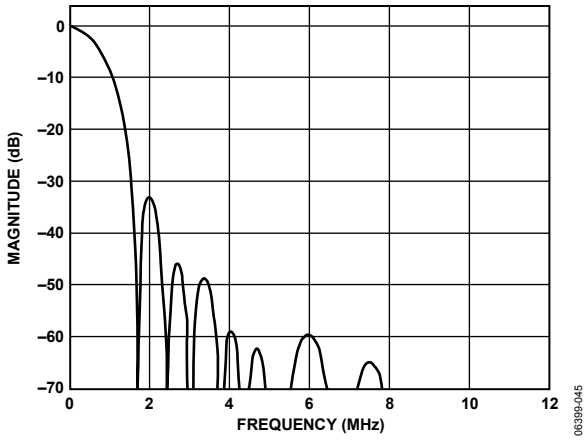


Figure 45. SD Chroma 0.65 MHz Low-Pass Filter Response

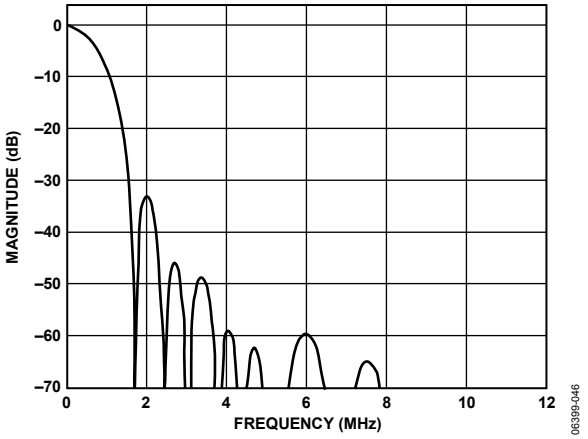


Figure 46. SD Chroma CIF Low-Pass Filter Response

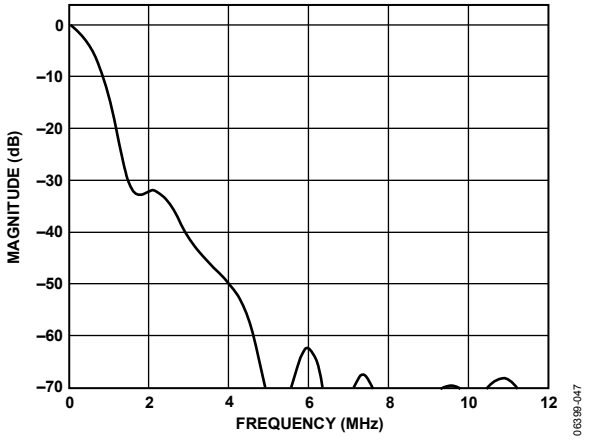


Figure 47. SD Chroma QCIF Low-Pass Filter Response

MPU PORT DESCRIPTION

Devices such as a microprocessor can communicate with the ADV7342/ADV7343 through one of the following protocols:

- 2-wire serial (I^2C-compatible) bus
- 4-wire serial (SPI-compatible) bus

After power-up or reset, the MPU port is configured for I^2C operation. SPI operation can be invoked at any time by following the procedure outlined in the SPI Operation section.

I^2C OPERATION

The ADV7342/ADV7343 support a 2-wire serial (I^2C-compatible) microprocessor bus driving multiple peripherals. This port operates in an open-drain configuration. Two inputs, serial data (SDA) and serial clock (SCL), carry information between any device connected to the bus and the ADV7342/ADV7343. Each slave device is recognized by a unique address. The ADV7342/ADV7343 have four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 48. The LSB either sets a read or write operation. Logic 1 corresponds to a read operation, while Logic 0 corresponds to a write operation. A1 is controlled by setting the ALSB/$\overline{\text{SPI\_SS}}$ pin of the ADV7342/ADV7343 to Logic 0 or Logic 1.

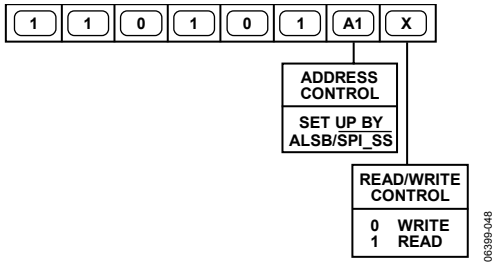


Figure 48. ADV7342 Slave Address = 0xD4 or 0xD6

To control the various devices on the bus, use the following protocol. The master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (7-bit address + R/$\overline{\text{W}}$ bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition occurs when the device monitors the SDA and SCL lines waiting for the start condition and the correct transmitted address. The R/$\overline{\text{W}}$ bit determines the direction of the data.

Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADV7342/ADV7343 act as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/$\overline{\text{W}}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. There is a subaddress auto-increment facility. This allows data to be written to or read from registers in ascending subaddress sequence starting at any valid subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCL high period, the user should issue only a start condition, a stop condition, or a stop condition followed by a start condition. If an invalid subaddress is issued by the user, the ADV7342/ADV7343 do not issue an acknowledge and do return to the idle condition. If the user utilizes the auto-increment method of addressing the encoder and exceeds the highest subaddress, the following actions are taken:

- In read mode, the highest subaddress register contents are output until the master device issues a no acknowledge. This indicates the end of a read. A no acknowledge condition occurs when the SDA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADV7342/ADV7343, and the parts return to the idle condition.

Figure 49 shows an example of data transfer for a write sequence and the start and stop conditions. Figure 50 shows bus write and read sequences.

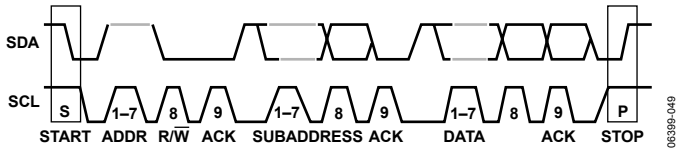


Figure 49. I²C Data Transfer

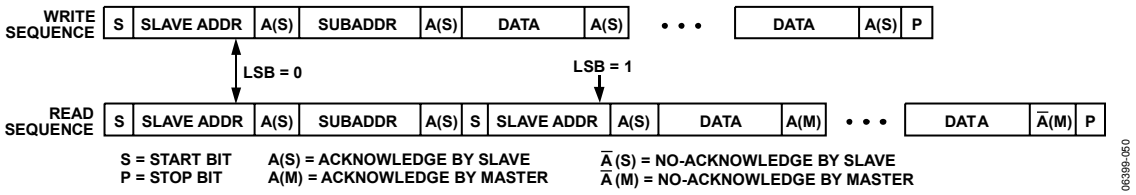


Figure 50. I²C Read and Write Sequence

SPI OPERATION

The ADV7342/ADV7343 support a 4-wire serial (SPI-compatible) bus connecting multiple peripherals. Two inputs, master out slave in (MOSI) and serial clock (SCLK), and one output, master in slave out (MISO), carry information between a master SPI peripheral on the bus and the ADV7342/ADV7343. Each slave device on the bus has a slave select pin that is connected to the master SPI peripheral by a unique slave select line. As such, slave device addressing is not required.

To invoke SPI operation, a master SPI peripheral (for example, a microprocessor) should issue three low pulses on the ADV7342/ADV7343 ALSB/$\overline{\text{SPI\_SS}}$ pin. When the encoder detects the third rising edge on the ALSB/$\overline{\text{SPI\_SS}}$ pin, it automatically switches to SPI communication mode. The ADV7342/ADV7343 remain in SPI communication mode until a reset or power-down occurs.

To control the ADV7342/ADV7343, use the following protocol for both read and write transactions. First, the master initiates a data transfer by driving and holding the ADV7342/ADV7343 ALSB/$\overline{\text{SPI\_SS}}$ pin low. On the first SCLK rising edge after ALSB/$\overline{\text{SPI\_SS}}$ has been driven low, the write command, defined as 0xD4, is written to the ADV7342/ADV7343 over the MOSI line. The second byte written to the MOSI line is interpreted as the starting subaddress. Data on the MOSI line is written MSB first and clocked on the rising edge of SCLK.

There is a subaddress auto-increment facility. This allows data to be written to or read from registers in ascending subaddress sequence starting at any valid subaddress. The user can also access any unique subaddress register on a one-by-one basis.

In a write data transfer, 8-bit data bytes are written to the ADV7342/ADV7343, MSB first, on the MOSI line immediately after the starting subaddress. The data bytes are clocked into the ADV7342/ADV7343 on the rising edge of SCLK. When all data bytes have been written, the master completes the transfer by driving and holding the ALSB/$\overline{\text{SPI\_SS}}$ pin high.

In a read data transfer, after the subaddress has been clocked in on the MOSI line, the ALSB/$\overline{\text{SPI\_SS}}$ pin is driven and held high for at least one clock cycle. Then, the ALSB/$\overline{\text{SPI\_SS}}$ pin is driven and held low again. On the first SCLK rising edge after ALSB/$\overline{\text{SPI\_SS}}$ has been driven low, the read command, defined as 0xD5, is written, MSB first, to the ADV7342/ADV7343 over the MOSI line. Subsequently, 8-bit data bytes are read from the ADV7342/ADV7343, MSB first, on the MISO line. The data bytes are clocked out of the ADV7342/ADV7343 on the falling edge of SCLK. When all data bytes have been read, the master completes the transfer by driving and holding the ALSB/$\overline{\text{SPI\_SS}}$ pin high.

REGISTER MAP ACCESS

A microprocessor can read from or write to all registers of the ADV7342/ADV7343 via the MPU port, except for registers that are specified as read-only or write-only registers.

The subaddress register determines which register the next read or write operation accesses. All communication through the MPU port starts with an access to the subaddress register. A read/write operation is then performed from/to the target address, which increments to the next address until the transaction is complete.

REGISTER PROGRAMMING

Table 14 to Table 28 describe the functionality of each register. All registers can be read from as well as written to, unless otherwise stated.

SUBADDRESS REGISTER (SR7 TO SR0)

The subaddress register is an 8-bit write-only register. After the MPU port is accessed and a read/write operation is selected, the subaddress is set up. The subaddress register determines to or from which register the operation takes place.

Table 14. Register 0x00

SR7 to SR0	Register	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0x00	Power Mode Register	Sleep Mode. With this control enabled, the current consumption is reduced to µA level. All DACs and the internal PLL circuit are disabled. I²C registers can be read from and written to in sleep mode.								0	Sleep mode off.	0x12
										1	Sleep mode on.	
		PLL and Oversampling Control. This control allows the internal PLL circuit to be powered down and the oversampling to be switched off.							0		PLL on.	
									1		PLL off.	
		DAC 3: Power on/off.						0			DAC 3 off.	
								1			DAC 3 on.	
		DAC 2: Power on/off.					0				DAC 2 off.	
							1				DAC 2 on.	
		DAC 1: Power on/off.				0					DAC 1 off.	
						1					DAC 1 on.	
		DAC 6: Power on/off.			0						DAC 6 off.	
					1						DAC 6 on.	
		DAC 5: Power on/off.		0							DAC 5 off.	
				1							DAC 5 on.	
		DAC 4: Power on/off.	0								DAC 4 off.	
			1								DAC 4 on.	

Table 15. Register 0x01 to Register 0x09

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x01	Mode Select Register	Reserved.								0		0x00
		DDR Clock Edge Alignment. Note: Only used for ED[1] and HD DDR modes.						0	0		Chroma clocked in on rising clock edge; luma clocked in on falling clock edge.	
								0	1		Reserved.	
								1	0		Reserved.	
								1	1		Luma clocked in on rising clock edge; chroma clocked in on falling clock edge.	
		Reserved.					0					
		Input Mode. Note: See Reg. 0x30, Bits[7:3] for ED/HD format selection.		0	0	0					SD input only.	
				0	0	1					ED/HD-SDR input only.	
				0	1	0					ED/HD-DDR input only.	
				0	1	1					SD and ED/HD-SDR.	
				1	0	0					SD and ED/HD-DDR.	
				1	0	1					Reserved.	
				1	1	0					Reserved.	
				1	1	1					ED only (at 54 MHz).	
		Y/C/S Bus Swap.	0								Allows data to be applied to data ports in various configurations (SD feature only).	
			1									
0x02	Mode Register 0	Reserved.							0	0	0 must be written to these bits.	0x20
		Test Pattern Black Bar.[2]						0			Disabled.	
								1			Enabled.	
		Manual CSC Matrix Adjust.					0				Disable manual CSC matrix adjust.	
							1				Enable manual CSC matrix adjust.	
		Sync on RGB.				0					No sync.	
						1					Sync on all RGB outputs.	
		RGB/YPrPb Output Select.			0						RGB component outputs.	
					1						YPrPb component outputs.	
		SD Sync Output Enable.		0							No sync output.	
				1							Output SD syncs on $\overline{\text{S\_HSYNC}}$ and $\overline{\text{S\_VSYNC}}$ pins.	
		ED/HD Sync Output Enable.	0								No sync output.	
			1								Output ED/HD syncs on $\overline{\text{S\_HSYNC}}$ and $\overline{\text{S\_VSYNC}}$ pins.	
0x03	ED/HD CSC Matrix 0								x	x	LSBs for GY.	0x03
0x04	ED/HD CSC Matrix 1								x	x	LSBs for RV.	0xF0
							x	x			LSBs for BU.	
					x	x					LSBs for GV.	
			x	x							LSBs for GU.	
0x05	ED/HD CSC Matrix 2		x	x	x	x	x	x	x	x	Bits[9:2] for GY.	0x4E
0x06	ED/HD CSC Matrix 3		x	x	x	x	x	x	x	x	Bits[9:2] for GU.	0x0E
0x07	ED/HD CSC Matrix 4		x	x	x	x	x	x	x	x	Bits[9:2] for GV.	0x24
0x08	ED/HD CSC Matrix 5		x	x	x	x	x	x	x	x	Bits[9:2] for BU.	0x92
0x09	ED/HD CSC Matrix 6		x	x	x	x	x	x	x	x	Bits[9:2] for RV.	0x7C

[1] ED = enhanced definition = 525p and 625p.
[2] Subaddress 0x31, Bit 2 must also be enabled (ED/HD). Subaddress 0x84, Bit 6 must also be enabled (SD).

Table 16. Register 0x0A to Register 0x10

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x0A	DAC 4, DAC 5, DAC 6 Output Levels	Positive Gain to DAC Output Voltage.	0	0	0	0	0	0	0	0	0%	0x00
			0	0	0	0	0	0	0	1	+0.018%	
			0	0	0	0	0	0	1	0	+0.036%	
			…	…	…	…	…	…	…	…	…	
			0	0	1	1	1	1	1	1	+7.382%	
			0	1	0	0	0	0	0	0	+7.5%	
		Negative Gain to DAC Output Voltage.	1	1	0	0	0	0	0	0	−7.5%	
			1	1	0	0	0	0	0	1	−7.382%	
			1	0	0	0	0	0	1	0	−7.364%	
			…	…	…	…	…	…	…	…	…	
			1	1	1	1	1	1	1	1	−0.018%	
0x0B	DAC 1, DAC 2, DAC 3 Output Levels	Positive Gain to DAC Output Voltage.	0	0	0	0	0	0	0	0	0%	0x00
			0	0	0	0	0	0	0	1	+0.018%	
			0	0	0	0	0	0	1	0	+0.036%	
			…	…	…	…	…	…	…	…	…	
			0	0	1	1	1	1	1	1	+7.382%	
			0	1	0	0	0	0	0	0	+7.5%	
		Negative Gain to DAC Output Voltage.	1	1	0	0	0	0	0	0	−7.5%	
			1	1	0	0	0	0	0	1	−7.382%	
			1	0	0	0	0	0	1	0	−7.364%	
			…	…	…	…	…	…	…	…	…	
			1	1	1	1	1	1	1	1	−0.018%	
0x0D	DAC Power Mode	DAC 1 Low Power Enable.								0	DAC 1 low power disabled	0x00
										1	DAC 1 low power enabled	
		DAC 2 Low Power Enable.							0		DAC 2 low power disabled	
									1		DAC 2 low power enabled	
		DAC 3 Low Power Enable.						0			DAC 3 low power disabled	
								1			DAC 3 low power enabled	
		Reserved.	0	0	0	0	0					
0x10	Cable Detection	DAC 1 Cable Detect (Read Only).								0	Cable detected on DAC 1	0x00
										1	DAC 1 unconnected	
		DAC 2 Cable Detect (Read Only).							0		Cable detected on DAC 2	
									1		DAC 2 unconnected	
		Reserved.					0	0				
		Unconnected DAC Auto Power-Down.				0					DAC auto power-down disable	
						1					DAC auto power-down enable	
		Reserved.	0	0	0							

Table 17. Register 0x12 to Register 0x17

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x12	Pixel Port Readback (S Bus)	S[7:0] Readback.	x	x	x	x	x	x	x	x	Read only	0xXX
0x13	Pixel Port Readback (Y Bus)	Y[7:0] Readback.	x	x	x	x	x	x	x	x	Read only	0xXX
0x14	Pixel Port Readback (C Bus)	C[7:0] Readback.	x	x	x	x	x	x	x	x	Read only	0xXX
0x16	Control Port Readback	$\overline{\text{P\_BLANK}}$.								x	Read only	0xXX
		$\overline{\text{P\_VSYNC}}$.							x			
		$\overline{\text{P\_HSYNC}}$.						x				
		$\overline{\text{S\_VSYNC}}$.					x					
		$\overline{\text{S\_HSYNC}}$.				x						
		SFL/MISO.			x							
		Reserved.	0	0								
0x17	Software Reset	Reserved.								0		0x00
		Software Reset.							0 1		Writing a 1 resets the device; this is a self-clearing bit	
		Reserved.	0	0	0	0	0	0				

Table 18. Register 0x30

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Note	Reset Value
0x30	ED/HD Mode Register 1	ED/HD Output Standard.							0	0	EIA770.2 output. EIA770.3 output.	ED HD	0x00
									0	1	EIA770.1 output		
									1	0	Output levels for full input range.		
									1	1	Reserved.		
		ED/HD Input Synchronization Format.						0			External $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ and field inputs.[1]		
								1			Embedded EAV/SAV codes.		
		ED/HD Input Mode.	0	0	0	0	0				SMPTE 293M, ITU-BT.1358.	525p @ 59.94 Hz	
			0	0	0	0	1				Nonstandard timing mode.		
			0	0	0	1	0				BTA-1004, ITU-BT.1362.	525p @ 59.94 Hz	
			0	0	0	1	1				ITU-BT.1358.	625p @ 50 Hz	
			0	0	1	0	0				ITU-BT.1362.	625p @ 50 Hz	
			0	0	1	0	1				SMPTE 296M-1, SMPTE 274M-2.	720p @ 60/59.94 Hz	
			0	0	1	1	0				SMPTE 296M-3.	720p @ 50 Hz	
			0	0	1	1	1				SMPTE 296M-4, SMPTE 274M-5.	720p @ 30/29.97 Hz	
			0	1	0	0	0				SMPTE 296M-6.	720p @ 25 Hz	
			0	1	0	0	1				SMPTE 296M-7, SMPTE 296M-8.	720p @ 24/23.98 Hz	
			0	1	0	1	0				SMPTE 240M.	1035i @ 60/59.94 Hz	
			0	1	0	1	1				Reserved.		
			0	1	1	0	0				Reserved.		
			0	1	1	0	1				SMPTE 274M-4, SMPTE 274M-5.	1080i @ 30/29.97 Hz	
			0	1	1	1	0				SMPTE 274M-6.	1080i @ 25 Hz	
			0	1	1	1	1				SMPTE 274M-7, SMPTE 274M-8.	1080p @ 0/29.97 Hz	
			1	0	0	0	0				SMPTE 274M-9.	1080p @ 25 Hz	
			1	0	0	0	1				SMPTE 274M-10, SMPTE 274M-11.	1080p @ 4/23.98 Hz	
			1	0	0	1	0				ITU-R BT.709-5.	1080Psf @ 24 Hz	
			10011–11111								Reserved.		

[1] Synchronization can be controlled with a combination of either $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs or $\overline{\text{HSYNC}}$ and field inputs, depending on Subaddress 0x34, Bit 6.

Table 19. Register 0x31 to Register 0x33

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x31	ED/HD Mode Register 2	ED/HD Pixel Data Valid.								0	Pixel data valid off.	0x00
										1	Pixel data valid on.	
		Reserved.							0			
		ED/HD Test Pattern Enable.						0			ED/HD test pattern off.	
								1			ED/HD test pattern on.	
		ED/HD Test Pattern Hatch/Field.					0				Hatch.	
							1				Field/frame.	
		ED/HD VBI Open.				0					Disabled.	
						1					Enabled.	
		ED/HD Undershoot Limiter.		0	0						Disabled.	
				0	1						−11 IRE	
				1	0						−6 IRE	
				1	1						−1.5 IRE	
		ED/HD Sharpness Filter.	0								Disabled.	
			1								Enabled.	
0x32	ED/HD Mode Register 3	ED/HD Y Delay with Respect to Falling Edge of HSYNC.						0	0	0	0 clock cycles.	0x00
								0	0	1	1 clock cycle.	
								0	1	0	2 clock cycles.	
								0	1	1	3 clock cycles.	
								1	0	0	4 clock cycles.	
		ED/HD Color Delay with Respect to Falling Edge of HSYNC.			0	0	0				0 clock cycles.	
					0	0	1				1 clock cycle.	
					0	1	0				2 clock cycles.	
					0	1	1				3 clock cycles.	
					1	0	0				4 clock cycles.	
		ED/HD CGMS.		0							Disabled.	
				1							Enabled.	
		ED/HD CGMS CRC.	0								Disabled.	
			1								Enabled.	
0x33	ED/HD Mode Register 4	ED/HD Cr/Cb Sequence.								0	Cb after falling edge of HSYNC.	0x68
										1	Cr after falling edge of HSYNC.	
		Reserved.						0	0		0 must be written to these bits.	
		Sinc Compensation Filter on DAC 1, DAC 2, DAC 3.					0				Disabled.	
							1				Enabled.	
		Reserved.				0					0 must be written to this bit.	
		ED/HD Chroma SSAF.			0						Disabled.	
					1						Enabled.	
		ED/HD Chroma Input.		0							4:4:4	
				1							4:2:2	
		ED/HD Double Buffering.	0								Disabled.	
			1								Enabled.	

Table 20. Register 0x34 to Register 0x35

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x34	ED/HD Mode Register 5	ED/HD Timing Reset.								0	Internal ED/HD timing counters enabled.	0x48
										1	Resets the internal ED/HD timing counters.	
		ED/HD $\overline{\text{HSYNC}}$ Control.[1]							0		$\overline{\text{HSYNC}}$ output control (refer to Table 51).	
									1			
		ED/HD $\overline{\text{VSYNC}}$ Control.[1]						0			$\overline{\text{VSYNC}}$ output control (refer to Table 52).	
								1				
		ED/HD Blank Polarity.					0				$\overline{\text{P\_BLANK}}$ active high.	
							1				$\overline{\text{P\_BLANK}}$ active low.	
		ED Macrovision Enable.				0					Macrovision disabled.	
						1					Macrovision enabled.	
		Reserved.			0						0 must be written to this bit.	
		ED/HD $\overline{\text{VSYNC}}$/Field Input.		0							0 = field input.	
				1							1 = $\overline{\text{VSYNC}}$ input.	
		Horizontal/Vertical Counters.[2]	0								Update field/line counter.	
			1								Field/line counter free running.	
0x35	ED/HD Mode Register 6	Reserved.								0		0x00
		ED/HD RGB Input Enable.							0		Disabled.	
									1		Enabled.	
		ED/HD Sync on PrPb.						0			Disabled.	
								1			Enabled.	
		ED/HD Color DAC Swap.					0				DAC 2 = Pb, DAC 3 = Pr.	
							1				DAC 2 = Pr, DAC 3 = Pb.	
		ED/HD Gamma Correction Curve Select.				0					Gamma Correction Curve A.	
						1					Gamma Correction Curve B.	
		ED/HD Gamma Correction Enable.			0						Disabled.	
					1						Enabled.	
		ED/HD Adaptive Filter Mode.		0							Mode A.	
				1							Mode B.	
		ED/HD Adaptive Filter Enable	0								Disabled.	
			1								Enabled.	

[1] Used in conjunction with ED/HD sync in Subaddress 0x02, Bit 7, set to 1.
[2] When set to 0, the horizontal/vertical counters automatically wrap around at the end of the line/field/frame of the selected standard. When set to 1, the horizontal/vertical counters are free running and wrap around when external sync signals indicate to do so.

Table 21. Register 0x36 to Register 0x43

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x36	ED/HD Y Level[1]	ED/HD Test Pattern Y Level.	x	x	x	x	x	x	x	x	Y level value	0xA0
0x37	ED/HD Cr Level[1]	ED/HD Test Pattern Cr Level.	x	x	x	x	x	x	x	x	Cr level value	0x80
0x38	ED/HD Cb Level[1]	ED/HD Test Pattern Cb Level.	x	x	x	x	x	x	x	x	Cb level value	0x80
0x39	ED/HD Mode Register 7	Reserved.				0	0	0	0	0		
		ED/HD EIA/CEA-861B Synchronization Compliance.			0 1						Disabled Enabled	
		Reserved.	0	0								
0x40	ED/HD Sharpness Filter Gain	ED/HD Sharpness Filter Gain, Value A.					0 0 … 0 1 … 1	0 0 … 1 0 … 1	0 0 … 1 0 … 1	0 1 … 1 0 … 1	Gain A = 0 Gain A = +1 … Gain A = +7 Gain A = −8 … Gain A = −1	0x00
		ED/HD Sharpness Filter Gain, Value B.	0 0 … 0 1 … 1	0 0 … 1 0 … 1	0 0 … 1 0 … 1	0 1 … 1 0 … 1					Gain B = 0 Gain B = +1 … Gain B = +7 Gain B = −8 … Gain B = −1	
0x41	ED/HD CGMS Data 0	ED/HD CGMS Data Bits.	0	0	0	0	C19	C18	C17	C16	CGMS C19 to C16	0x00
0x42	ED/HD CGMS Data 1	ED/HD CGMS Data Bits.	C15	C14	C13	C12	C11	C10	C9	C8	CGMS C15 to C8	0x00
0x43	ED/HD CGMS Data 2	ED/HD CGMS Data Bits.	C7	C6	C5	C4	C3	C2	C1	C0	CGMS C7 to C0	0x00

[1] For use with ED/HD internal test patterns only (Subaddress 0x31, Bit 2 = 1).

Table 22. Register 0x44 to Register 0x57

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x44	ED/HD Gamma A0	ED/HD Gamma Curve A (Point 24).	x	x	x	x	x	x	x	x	A0	0x00
0x45	ED/HD Gamma A1	ED/HD Gamma Curve A (Point 32).	x	x	x	x	x	x	x	x	A1	0x00
0x46	ED/HD Gamma A2	ED/HD Gamma Curve A (Point 48).	x	x	x	x	x	x	x	x	A2	0x00
0x47	ED/HD Gamma A3	ED/HD Gamma Curve A (Point 64).	x	x	x	x	x	x	x	x	A3	0x00
0x48	ED/HD Gamma A4	ED/HD Gamma Curve A (Point 80).	x	x	x	x	x	x	x	x	A4	0x00
0x49	ED/HD Gamma A5	ED/HD Gamma Curve A (Point 96).	x	x	x	x	x	x	x	x	A5	0x00
0x4A	ED/HD Gamma A6	ED/HD Gamma Curve A (Point 128).	x	x	x	x	x	x	x	x	A6	0x00
0x4B	ED/HD Gamma A7	ED/HD Gamma Curve A (Point 160).	x	x	x	x	x	x	x	x	A7	0x00
0x4C	ED/HD Gamma A8	ED/HD Gamma Curve A (Point 192).	x	x	x	x	x	x	x	x	A8	0x00
0x4D	ED/HD Gamma A9	ED/HD Gamma Curve A (Point 224).	x	x	x	x	x	x	x	x	A9	0x00
0x4E	ED/HD Gamma B0	ED/HD Gamma Curve B (Point 24).	x	x	x	x	x	x	x	x	B0	0x00
0x4F	ED/HD Gamma B1	ED/HD Gamma Curve B (Point 32).	x	x	x	x	x	x	x	x	B1	0x00
0x50	ED/HD Gamma B2	ED/HD Gamma Curve B (Point 48).	x	x	x	x	x	x	x	x	B2	0x00
0x51	ED/HD Gamma B3	ED/HD Gamma Curve B (Point 64).	x	x	x	x	x	x	x	x	B3	0x00
0x52	ED/HD Gamma B4	ED/HD Gamma Curve B (Point 80).	x	x	x	x	x	x	x	x	B4	0x00
0x53	ED/HD Gamma B5	ED/HD Gamma Curve B (Point 96).	x	x	x	x	x	x	x	x	B5	0x00
0x54	ED/HD Gamma B6	ED/HD Gamma Curve B (Point 128).	x	x	x	x	x	x	x	x	B6	0x00
0x55	ED/HD Gamma B7	ED/HD Gamma Curve B (Point 160).	x	x	x	x	x	x	x	x	B7	0x00
0x56	ED/HD Gamma B8	ED/HD Gamma Curve B (Point 192).	x	x	x	x	x	x	x	x	B8	0x00
0x57	ED/HD Gamma B9	ED/HD Gamma Curve B (Point 224).	x	x	x	x	x	x	x	x	B9	0x00

Table 23. Register 0x58 to Register 0x5D

SR7 to SR0	Register	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0x58	ED/HD Adaptive Filter Gain 1	ED/HD Adaptive Filter Gain 1, Value A.					0	0	0	0	Gain A = 0	0x00
							0	0	0	1	Gain A = +1	
							…	…	…	…	…	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = −8	
							…	…	…	…	…	
							1	1	1	1	Gain A = −1	
		ED/HD Adaptive Filter Gain 1, Value B.	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			…	…	…	…					…	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = −8	
			…	…	…	…					…	
			1	1	1	1					Gain B = −1	
0x59	ED/HD Adaptive Filter Gain 2	ED/HD Adaptive Filter Gain 2, Value A.					0	0	0	0	Gain A = 0	0x00
							0	0	0	1	Gain A = +1	
							…	…	…	…	…	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = −8	
							…	…	…	…	…	
							1	1	1	1	Gain A = −1	
		ED/HD Adaptive Filter Gain 2, Value B.	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			…	…	…	…					…	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = −8	
			…	…	…	…					…	
			1	1	1	1					Gain B = −1	
0x5A	ED/HD Adaptive Filter Gain 3	ED/HD Adaptive Filter Gain 3, Value A.					0	0	0	0	Gain A = 0	0x00
							0	0	0	1	Gain A = +1	
							…	…	…	…	…	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = −8	
							…	…	…	…	…	
							1	1	1	1	Gain A = −1	
		ED/HD Adaptive Filter Gain 3, Value B.	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			…	…	…	…					…	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = −8	
			…	…	…	…					…	
			1	1	1	1					Gain B = −1	
0x5B	ED/HD Adaptive Filter Threshold A	ED/HD Adaptive Filter Threshold A.	x	x	x	x	x	x	x	x	Threshold A	0x00
0x5C	ED/HD Adaptive Filter Threshold B	ED/HD Adaptive Filter Threshold B.	x	x	x	x	x	x	x	x	Threshold B	0x00
0x5D	ED/HD Adaptive Filter Threshold C	ED/HD Adaptive Filter Threshold C.	x	x	x	x	x	x	x	x	Threshold C	0x00

Table 24. Register 0x5E to Register 0x6E

SR7 to SR0	Register	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0x5E	ED/HD CGMS Type B Register 0	ED/HD CGMS Type B Enable.								0 1	Disabled Enabled	0x00
		ED/HD CGMS Type B CRC Enable.							0 1		Disabled Enabled	
		ED/HD CGMS Type B Header Bits.	H5	H4	H3	H2	H1	H0			H5 to H0	
0x5F	ED/HD CGMS Type B Register 1	ED/HD CGMS Type B Data Bits.	P7	P6	P5	P4	P3	P2	P1	P0	P7 to P0	0x00
0x60	ED/HD CGMS Type B Register 2	ED/HD CGMS Type B Data Bits.	P15	P14	P13	P12	P11	P10	P9	P8	P15 to P8	0x00
0x61	ED/HD CGMS Type B Register 3	ED/HD CGMS Type B Data Bits.	P23	P22	P21	P20	P19	P18	P17	P16	P23 to P16	0x00
0x62	ED/HD CGMS Type B Register 4	ED/HD CGMS Type B Data Bits.	P31	P30	P29	P28	P27	P26	P25	P24	P31 to P24	0x00
0x63	ED/HD CGMS Type B Register 5	ED/HD CGMS Type B Data Bits.	P39	P38	P37	P36	P35	P34	P33	P32	P39 to P32	0x00
0x64	ED/HD CGMS Type B Register 6	ED/HD CGMS Type B Data Bits.	P47	P46	P45	P44	P43	P42	P41	P40	P47 to P40	0x00
0x65	ED/HD CGMS Type B Register 7	ED/HD CGMS Type B Data Bits.	P55	P54	P53	P52	P51	P50	P49	P48	P55 to P48	0x00
0x66	ED/HD CGMS Type B Register 8	ED/HD CGMS Type B Data Bits.	P63	P62	P61	P60	P59	P58	P57	P56	P63 to P56	0x00
0x67	ED/HD CGMS Type B Register 9	ED/HD CGMS Type B Data Bits.	P71	P70	P69	P68	P67	P66	P65	P64	P71 to P64	0x00
0x68	ED/HD CGMS Type B Register 10	ED/HD CGMS Type B Data Bits.	P79	P78	P77	P76	P75	P74	P73	P72	P79 to P72	0x00
0x69	ED/HD CGMS Type B Register 11	ED/HD CGMS Type B Data Bits.	P87	P86	P85	P84	P83	P82	P81	P80	P87 to P80	0x00
0x6A	ED/HD CGMS Type B Register 12	ED/HD CGMS Type B Data Bits.	P95	P94	P93	P92	P91	P90	P89	P88	P95 to P88	0x00
0x6B	ED/HD CGMS Type B Register 13	ED/HD CGMS Type B Data Bits.	P103	P102	P101	P100	P99	P98	P97	P96	P103 to P96	0x00
0x6C	ED/HD CGMS Type B Register 14	ED/HD CGMS Type B Data Bits.	P111	P110	P109	P108	P107	P106	P105	P104	P111 to P104	0x00
0x6D	ED/HD CGMS Type B Register 15	ED/HD CGMS Type B Data Bits.	P119	P118	P117	P116	P115	P114	P113	P112	P119 to P112	0x00
0x6E	ED/HD CGMS Type B Register 16	ED/HD CGMS Type B Data Bits.	P127	P126	P125	P124	P123	P122	P121	P120	P127 to P120	0x00

Table 25. Register 0x80 to Register 0x83

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x80	SD Mode Register 1	SD Standard.							0	0	NTSC.	0x10
									0	1	PAL B/D/G/H/I.	
									1	0	PAL M.	
									1	1	PAL N.	
		SD Luma Filter.				0	0	0			LPF NTSC.	
						0	0	1			LPF PAL.	
						0	1	0			Notch NTSC.	
						0	1	1			Notch PAL.	
						1	0	0			SSAF luma.	
						1	0	1			Luma CIF.	
						1	1	0			Luma QCIF.	
						1	1	1			Reserved.	
		SD Chroma Filter.	0	0	0						1.3 MHz.	
			0	0	1						0.65 MHz.	
			0	1	0						1.0 MHz.	
			0	1	1						2.0 MHz.	
			1	0	0						Reserved.	
			1	0	1						Chroma CIF.	
			1	1	0						Chroma QCIF.	
			1	1	1						3.0 MHz.	
0x82	SD Mode Register 2	SD PrPb SSAF.								0	Disabled.	0x0B
										1	Enabled.	
		SD DAC Output 1.							0		Refer to Table 32 in the Output Configuration section.	
									1			
		SD DAC Output 2.						0			Refer to Table 32 in the Output Configuration section.	
								1				
		SD Pedestal.					0				Disabled.	
							1				Enabled.	
		SD Square Pixel Mode.				0					Disabled.	
						1					Enabled.	
		SD VCR FF/RW Sync.			0						Disabled.	
					1						Enabled.	
		SD Pixel Data Valid.		0							Disabled.	
				1							Enabled.	
		SD Active Video Edge Control.	0								Disabled.	
			1								Enabled.	
0x83	SD Mode Register 3	SD Pedestal on YPrPb Output.								0	No pedestal on YPrPb.	0x04
										1	7.5 IRE pedestal on YPrPb.	
		SD Output Levels Y.							0		Y = 700 mV/300 mV.	
									1		Y = 714 mV/286 mV.	
		SD Output Levels PrPb.					0	0			700 mV p-p (PAL), 1000 mV p-p (NTSC).	
							0	1			700 mV p-p.	
							1	0			1000 mV p-p.	
							1	1			648 mV p-p.	
		SD VBI Open.				0					Disabled.	
						1					Enabled.	
		SD Closed Captioning Field Control.		0	0						Closed captioning disabled.	
				0	1						Closed captioning on odd field only.	
				1	0						Closed captioning on even field only.	
				1	1						Closed captioning on both fields.	
		Reserved.	0								Reserved.	

Table 26. Register 0x84 to Register 0x89

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x84	SD Mode Register 4	SD $\overline{\text{VSYNC}}$-3H.								0	Disabled.	0x00
										1	$\overline{\text{VSYNC}}$ = 2.5 lines (PAL), $\overline{\text{VSYNC}}$ = 3 lines (NTSC).	
		SD SFL/SCR/TR Mode Select.						0	0		Disabled.	
								0	1		Subcarrier phase reset mode enabled.	
								1	0		Timing reset mode enabled.	
								1	1		SFL mode enabled.	
		SD Active Video Length.					0				720 pixels.	
							1				710 (NTSC), 702 (PAL).	
		SD Chroma.				0					Chroma enabled.	
						1					Chroma disabled.	
		SD Burst.			0						Enabled.	
					1						Disabled.	
		SD Color Bars.		0							Disabled.	
				1							Enabled.	
		SD Luma/Chroma Swap.	0								DAC 2 = luma, DAC 3 = chroma.	
			1								DAC 2 = chroma, DAC 3 = luma.	
0x86	SD Mode Register 5	NTSC Color Subcarrier Adjust (Delay from the falling edge of output HSYNC pulse to start of color burst).							0	0	5.17 µs.	0x02
									0	1	5.31 µs.	
									1	0	5.59 µs (must be set for Macrovision compliance).	
									1	1	Reserved.	
		Reserved.						0				
		SD EIA/CEA-861B Synchronization Compliance.					0				Disabled.	
							1				Enabled.	
		Reserved.			0	0						
		SD Horizontal/Vertical Counter Mode.[1]		0							Update field/line counter.	
				1							Field/line counter free running.	
		SD RGB Color Swap.	0								Normal.	
			1								Color reversal enabled.	
0x87	SD Mode Register 6	SD PrPb Scale.								0	Disabled.	0x00
										1	Enabled.	
		SD Y Scale.							0		Disabled.	
									1		Enabled.	
		SD Hue Adjust.						0			Disabled.	
								1			Enabled.	
		SD Brightness.					0				Disabled.	
							1				Enabled.	
		SD Luma SSAF Gain.				0					Disabled.	
						1					Enabled.	
		SD Input Standard Auto Detect.			0						Disabled.	
					1						Enabled.	
		Reserved.		0							0 must be written to this bit.	
		SD RGB Input Enable.	0								SD YCrCb input.	
			1								SD RGB input.	

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x88	SD Mode Register 7	Reserved.								0		0x00
		SD Noninterlaced Mode.							0		Disabled.	
									1		Enabled.	
		SD Double Buffering.						0			Disabled.	
								1			Enabled.	
		SD Input Format.				0	0				8-bit input.	
						0	1				16-bit input.	
						1	0				Reserved.	
						1	1				Reserved.	
		SD Digital Noise Reduction.			0						Disabled.	
					1						Enabled.	
		SD Gamma Correction Enable.		0							Disabled.	
				1							Enabled.	
		SD Gamma Correction Curve Select.	0								Gamma Correction Curve A.	
			1								Gamma Correction Curve B.	
0x89	SD Mode Register 8	SD Undershoot Limiter.							0	0	Disabled.	0x00
									0	1	−11 IRE.	
									1	0	−6 IRE.	
									1	1	−1.5 IRE.	
		Reserved.						0			0 must be written to this bit.	
		SD Black Burst Output on DAC Luma.					0				Disabled.	
							1				Enabled.	
		SD Chroma Delay.			0	0					Disabled.	
					0	1					4 clock cycles.	
					1	0					8 clock cycles.	
					1	1					Reserved.	
		Reserved.	0	0							0 must be written to these bits.	

[1] When set to 0, the horizontal/vertical counters automatically wrap around at the end of the line/field/frame of the selected standard. When set to 1, the horizontal/vertical counters are free running and wrap around when external sync signals indicate to do so.

Table 27. Register 0x8A to Register 0x98

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x8A	SD Timing Register 0	SD Slave/Master Mode.								0	Slave mode.	0x08
										1	Master mode.	
		SD Timing Mode.						0	0		Mode 0.	
								0	1		Mode 1.	
								1	0		Mode 2.	
								1	1		Mode 3.	
		Reserved.					1					
		SD Luma Delay.			0	0					No delay.	
					0	1					2 clock cycles.	
					1	0					4 clock cycles.	
					1	1					6 clock cycles.	
		SD Minimum Luma Value.		0							−40 IRE.	
				1							−7.5 IRE.	
		SD Timing Reset.	x								A low-high-low transition resets the internal SD timing counters.	
0x8B	SD Timing Register 1 (Note: Applicable in master modes only, that is, Subaddress 0x8A, Bit 0 = 1)	SD $\overline{\text{HSYNC}}$ Width.							0	0	t_a = 1 clock cycle.	0x00
									0	1	t_a = 4 clock cycles.	
									1	0	t_a = 16 clock cycles.	
									1	1	t_a = 128 clock cycles.	
		SD $\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$ Delay.					0	0			t_b = 0 clock cycles.	
							0	1			t_b = 4 clock cycles.	
							1	0			t_b = 8 clock cycles.	
							1	1			t_b = 18 clock cycles.	
		SD $\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$ Rising Edge Delay (Mode 1 Only).			x	0					$t_c = t_b$.	
					x	1					$t_c = t_b$ + 32 µs.	
		SD $\overline{\text{VSYNC}}$ Width (Mode 2 Only).			0	0					1 clock cycle.	
					0	1					4 clock cycles.	
					1	0					16 clock cycles.	
					1	1					128 clock cycles.	
		SD $\overline{\text{HSYNC}}$ to Pixel Data Adjust.	0	0							0 clock cycles.	
			0	1							1 clock cycle.	
			1	0							2 clock cycles.	
			1	1							3 clock cycles.	
0x8C	SD F_{SC} Register 0[1]	Subcarrier Frequency Bits[7:0].	x	x	x	x	x	x	x	x	Subcarrier Frequency Bits[7:0].	0x1F
0x8D	SD F_{SC} Register 1[1]	Subcarrier Frequency Bits[15:8].	x	x	x	x	x	x	x	x	Subcarrier Frequency Bits[15:8].	0x7C
0x8E	SD F_{SC} Register 2[1]	Subcarrier Frequency Bits[23:16].	x	x	x	x	x	x	x	x	Subcarrier Frequency Bits[23:16].	0xF0
0x8F	SD F_{SC} Register 3[1]	Subcarrier Frequency Bits[31:24].	x	x	x	x	x	x	x	x	Subcarrier Frequency Bits[31:24].	0x21
0x90	SD F_{SC} Phase	Subcarrier Phase Bits[9:2].	x	x	x	x	x	x	x	x	Subcarrier Phase Bits[9:2].	0x00
0x91	SD Closed Captioning	Extended Data on Even Fields.	x	x	x	x	x	x	x	x	Extended Data Bits[7:0].	0x00
0x92	SD Closed Captioning	Extended Data on Even Fields.	x	x	x	x	x	x	x	x	Extended Data Bits[15:8].	0x00
0x93	SD Closed Captioning	Data on Odd Fields.	x	x	x	x	x	x	x	x	Data Bits[7:0].	0x00
0x94	SD Closed Captioning	Data on Odd Fields.	x	x	x	x	x	x	x	x	Data Bits[15:8].	0x00
0x95	SD Pedestal Register 0	Pedestal on Odd Fields.	17	16	15	14	13	12	11	10	Setting any of these bits to 1 disables pedestal on the line number indicated by the bit settings.	0x00
0x96	SD Pedestal Register 1	Pedestal on Odd Fields.	25	24	23	22	21	20	19	18		0x00
0x97	SD Pedestal Register 2	Pedestal on Even Fields.	17	16	15	14	13	12	11	10		0x00
0x98	SD Pedestal Register 3	Pedestal on Even Fields.	25	24	23	22	21	20	19	18		0x00

[1] SD subcarrier frequency registers default to NTSC subcarrier frequency values.

Table 28. Register 0x99 to Register 0xA5

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0x99	SD CGMS/WSS 0	SD CGMS Data.					x	x	x	x	CGMS Data Bits[C19:C16]	0x00
		SD CGMS CRC.				0					Disabled	
						1					Enabled	
		SD CGMS on Odd Fields.			0						Disabled	
					1						Enabled	
		SD CGMS on Even Fields.		0							Disabled	
				1							Enabled	
		SD WSS.	0								Disabled	
			1								Enabled	
0x9A	SD CGMS/WSS 1	SD CGMS/WSS Data.			x	x	x	x	x	x	CGMS Data Bits[C13:C8] or WSS Data Bits[W13:W8]	0x00
		SD CGMS Data.	x	x							CGMS Data Bits[C15:C14]	
0x9B	SD CGMS/WSS 2	SD CGMS/WSS Data.	x	x	x	x	x	x	x	x	CGMS Data Bits[C7:C0] or WSS Data Bits[W7:W0]	0x00
0x9C	SD Scale LSB Register	LSBs for SD Y Scale Value.							x	x	SD Y Scale Bits[1:0]	0x00
		LSBs for SD Cb Scale Value.					x	x			SD Cb Scale Bits[1:0]	
		LSBs for SD Cr Scale Value.			x	x					SD Cr Scale Bits[1:0].	
		LSBs for SD F_{SC} Phase.	x	x							Subcarrier Phase Bits[1:0]	
0x9D	SD Y Scale Register	SD Y Scale Value.	x	x	x	x	x	x	x	x	SD Y Scale Bits[9:2]	0x00
0x9E	SD Cb Scale Register	SD Cb Scale Value.	x	x	x	x	x	x	x	x	SD Cb Scale Bits[9:2]	0x00
0x9F	SD Cr Scale Register	SD Cr Scale Value.	x	x	x	x	x	x	x	x	SD Cr Scale Bits[9:2]	0x00
0xA0	SD Hue Register	SD Hue Adjust Value.	x	x	x	x	x	x	x	x	SD Hue Adjust Bits[7:0]	0x00
0xA1	SD Brightness/WSS	SD Brightness Value.		x	x	x	x	x	x	x	SD Brightness Bits[6:0]	0x00
		SD Blank WSS Data.	0								Disabled	
			1								Enabled	
0xA2	SD Luma SSAF	SD Luma SSAF Gain/Attenuation. Note: Only applicable if Register 0x87, Bit 4 = 1.					0	0	0	0	−4 dB	0x00
							…	…	…	…	…	
							0	1	1	0	0 dB	
							…	…	…	…	…	
							1	1	0	0	+4 dB	
		Reserved.	0	0	0	0						
0xA3	SD DNR 0	Coring Gain Border. Note: In DNR mode, the values in brackets apply.					0	0	0	0	No gain	0x00
							0	0	0	1	+1/16 [−1/8]	
							0	0	1	0	+2/16 [−2/8]	
							0	0	1	1	+3/16 [−3/8]	
							0	1	0	0	+4/16 [−4/8]	
							0	1	0	1	+5/16 [−5/8]	
							0	1	1	0	+6/16 [−6/8]	
							0	1	1	1	+7/16 [−7/8]	
							1	0	0	0	+8/16 [−1]	
		Coring Gain Data. Note: In DNR mode, the values in brackets apply.	0	0	0	0					No gain	
			0	0	0	1					+1/16 [−1/8]	
			0	0	1	0					+2/16 [−2/8]	
			0	0	1	1					+3/16 [−3/8]	
			0	1	0	0					+4/16 [−4/8]	
			0	1	0	1					+5/16 [−5/8]	
			0	1	1	0					+6/16 [−6/8]	
			0	1	1	1					+7/16 [−7/8]	
			1	0	0	0					+8/16 [−1]	

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0xA4	SD DNR 1	DNR Threshold.			0	0	0	0	0	0	0	0x00
					0	0	0	0	0	1	1	
					…	…	…	…	…	…	…	
					1	1	1	1	1	0	62	
					1	1	1	1	1	1	63	
		Border Area.		0							2 pixels	
				1							4 pixels	
		Block Size Control.	0								8 pixels	
			1								16 pixels	
0xA5	SD DNR 2	DNR Input Select.						0	0	1	Filter A	0x00
								0	1	0	Filter B	
								0	1	1	Filter C	
								1	0	0	Filter D	
		DNR Mode.					0				DNR mode	
							1				DNR sharpness mode	
		DNR Block Offset.	0	0	0	0					0 pixel offset	
			0	0	0	1					1 pixel offset	
			…	…	…	…					…	
			1	1	1	0					14 pixel offset	
			1	1	1	1					15 pixel offset	

Table 29. Register 0xA6 to Register 0xBB

SR7 to SR0	Register	Bit Description	Bit Number 7	6	5	4	3	2	1	0	Register Setting	Reset Value
0xA6	SD Gamma A 0	SD Gamma Curve A (Point 24).	x	x	x	x	x	x	x	x	A0	0x00
0xA7	SD Gamma A 1	SD Gamma Curve A (Point 32).	x	x	x	x	x	x	x	x	A1	0x00
0xA8	SD Gamma A 2	SD Gamma Curve A (Point 48).	x	x	x	x	x	x	x	x	A2	0x00
0xA9	SD Gamma A 3	SD Gamma Curve A (Point 64).	x	x	x	x	x	x	x	x	A3	0x00
0xAA	SD Gamma A 4	SD Gamma Curve A (Point 80).	x	x	x	x	x	x	x	x	A4	0x00
0xAB	SD Gamma A 5	SD Gamma Curve A (Point 96).	x	x	x	x	x	x	x	x	A5	0x00
0xAC	SD Gamma A 6	SD Gamma Curve A (Point 128).	x	x	x	x	x	x	x	x	A6	0x00
0xAD	SD Gamma A 7	SD Gamma Curve A (Point 160).	x	x	x	x	x	x	x	x	A7	0x00
0xAE	SD Gamma A 8	SD Gamma Curve A (Point 192).	x	x	x	x	x	x	x	x	A8	0x00
0xAF	SD Gamma A 9	SD Gamma Curve A (Point 224).	x	x	x	x	x	x	x	x	A9	0x00
0xB0	SD Gamma B 0	SD Gamma Curve B (Point 24).	x	x	x	x	x	x	x	x	B0	0x00
0xB1	SD Gamma B 1	SD Gamma Curve B (Point 32).	x	x	x	x	x	x	x	x	B1	0x00
0xB2	SD Gamma B 2	SD Gamma Curve B (Point 48).	x	x	x	x	x	x	x	x	B2	0x00
0xB3	SD Gamma B 3	SD Gamma Curve B (Point 64).	x	x	x	x	x	x	x	x	B3	0x00
0xB4	SD Gamma B 4	SD Gamma Curve B (Point 80).	x	x	x	x	x	x	x	x	B4	0x00
0xB5	SD Gamma B 5	SD Gamma Curve B (Point 96).	x	x	x	x	x	x	x	x	B5	0x00
0xB6	SD Gamma B 6	SD Gamma Curve B (Point 128).	x	x	x	x	x	x	x	x	B6	0x00
0xB7	SD Gamma B 7	SD Gamma Curve B (Point 160).	x	x	x	x	x	x	x	x	B7	0x00
0xB8	SD Gamma B 8	SD Gamma Curve B (Point 192).	x	x	x	x	x	x	x	x	B8	0x00
0xB9	SD Gamma B 9	SD Gamma Curve B (Point 224).	x	x	x	x	x	x	x	x	B9	0x00
0xBA	SD Brightness Detect	SD Brightness Value.	x	x	x	x	x	x	x	x	Read only.	0xXX
0xBB	Field Count Register	Field Count.						x	x	x	Read only.	0x0X
		Reserved.			0	0	0				Reserved.	
		Revision Code.	0	0							Read only.	

Table 30. Register 0xE0 to Register 0xF1

SR7 to SR0	Register[1]	Bit Description	Bit Number								Register Setting	Reset Value
			7	6	5	4	3	2	1	0		
0xE0	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xE1	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xE2	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xE3	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xE4	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xE5	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xE6	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xE7	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xE8	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xE9	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xEA	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xEB	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xEC	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xED	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xEE	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xEF	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xF0	Macrovision	MV Control Bits.	x	x	x	x	x	x	x	x		0x00
0xF1	Macrovision	MV Control Bit.	0	0	0	0	0	0	0	x	Bits[7:1] must be 0.	0x00

[1] Macrovision registers are available on the ADV7342 only.

INPUT CONFIGURATION

The ADV7342/ADV7343 support a number of different input modes. The desired input mode is selected using Subaddress 0x01, Bits[6:4]. The ADV7342/ADV7343 default to standard definition only (SD only) upon power-up. Table 31 provides an overview of all possible input configurations. Each input mode is described in detail in the following sections.

STANDARD DEFINITION ONLY

Subaddress 0x01, Bits[6:4] = 000

Standard definition (SD) YCrCb data can be input in 4:2:2 format. Standard definition (SD) RGB data can be input in 4:4:4 format.

A 27 MHz clock signal must be provided on the CLKIN_A pin. Input synchronization signals are provided on the S_HSYNC and S_VSYNC pins.

8-Bit 4:2:2 YCrCb Mode

Subaddress 0x87, Bit 7 = 0; Subaddress 0x88, Bit 3 = 0

In 8-bit 4:2:2 YCrCb input mode, the interleaved pixel data is input on Pin S7 to Pin S0 (or Pin Y7 to Pin Y0, depending on Subaddress 0x01, Bit 7), with S0/Y0 being the LSB. The ITU-R BT.601/656 input standard is supported.

16-Bit 4:2:2 YCrCb Mode

Subaddress 0x87, Bit 7 = 0; Subaddress 0x88, Bit 3 = 1

In 16-bit 4:2:2 YCrCb input mode, the Y pixel data is input on Pin S7 to Pin S0 (or Pin Y7 to Pin Y0, depending on Subaddress 0x01, Bit 7), with S0/Y0 being the LSB.

The CrCb pixel data is input on Pin Y7 to Pin Y0 (or Pin C7 to Pin C0, depending on Subaddress 0x01, Bit 7), with Y0/C0 being the LSB.

24-Bit 4:4:4 RGB Mode

Subaddress 0x87, Bit 7 = 1

In 24-bit 4:4:4 RGB input mode, the red pixel data is input on Pin S7 to Pin S0, the green pixel data is input on Pin Y7 to Pin Y0, and the blue pixel data is input on Pin C7 to Pin C0. S0, Y0, and C0 are the respective bus LSBs.

Table 31. Input Configuration

Input Mode[1]		S								Y								C							
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
000	SD Only	Y/C/S Bus Swap (0x01[7]) = 0																							
	8-Bit YCrCb[2]	YCrCb																							
	16-Bit YCrCb[2, 3]	Y								CrCb															
		Y/C/S Bus Swap (0x01[7]) = 1																							
	8-Bit YCrCb[2]									YCrCb															
	16-Bit YCrCb[2, 3]									Y								CrCb							
		SD RGB Input Enable (0x87[7]) = 1																							
	24-Bit RGB[3]	R								G								B							
001	ED/HD-SDR Only[4, 5]	ED/HD RGB Input Enable (0x35[1]) = 0																							
	16-Bit YCrCb									Y								CrCb							
	24-Bit YCrCb	Cr								Y								Cb							
		ED/HD RGB Input Enable (0x35[1]) = 1																							
	24-Bit RGB[3]	R								G								B							
010	ED/HD-DDR Only (8-Bit)[5]									YCrCb															
011	SD and ED/HD-SDR (24-Bit)[5]	YCrCb (SD)								Y (ED/HD)								CrCb (ED/HD)							
100	SD and ED/HD-DDR (16-Bit)[5]	YCrCb (SD)								YCrCb (ED/HD)															
111	ED Only (54 MHz) (8-Bit)[5]									YCrCb															

[1] The input mode is determined by Subaddress 0x01, Bits[6:4].
[2] In SD only (YCrCb) mode, the format of the input data is determined by Subaddress 0x88, Bits[4:3]. See Table 26 for more information.
[3] External synchronization signals must be used in this input mode. Embedded EAV/SAV timing codes are not supported.
[4] In ED/HD-SDR only (YCrCb) mode, the format of the input data is determined by Subaddress 0x33, Bit 6. See Table 19 for more information.
[5] ED = enhanced definition = 525p and 625p.

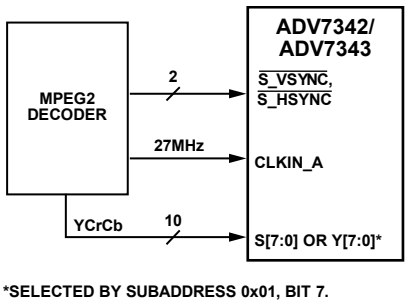


Figure 51. SD Only Example Application

ENHANCED DEFINITION/HIGH DEFINITION ONLY

Subaddress 0x01, Bits[6:4] = 001 or 010

Enhanced definition (ED) or high definition (HD) YCrCb data can be input in either 4:2:2 or 4:4:4 formats. If desired, dual data rate (DDR) pixel data inputs can be employed (4:2:2 format only).

Enhanced definition (ED) or high definition (HD) RGB data can be input in 4:4:4 format (single data rate only).

The clock signal must be provided on the CLKIN_A pin. Input synchronization signals are provided on the P_HSYNC, P_VSYNC, and P_BLANK pins.

16-Bit 4:2:2 YCrCb Mode (SDR)

Subaddress 0x35, Bit 1 = 0; Subaddress 0x33, Bit 6 = 1

In 16-bit 4:2:2 YCrCb input mode, the Y pixel data is input on Pin Y7 to Pin Y0, with Y0 being the LSB.

The CrCb pixel data is input on Pin C7 to Pin C0, with C0 being the LSB.

8-Bit 4:2:2 YCrCb Mode (DDR)

Subaddress 0x35, Bit 1 = 0; Subaddress 0x33, Bit 6 = 1

In 8-bit DDR 4:2:2 YCrCb input mode, the Y pixel data is input on Pin Y7 to Pin Y0 upon either the rising or falling edge of CLKIN_A. Y0 is the LSB.

The CrCb pixel data is also input on Pin Y7 to Pin Y0 upon the opposite edge of CLKIN_A. Y0 is the LSB.

Whether the Y data is clocked in upon the rising or falling edge of CLKIN_A is determined by Subaddress 0x01, Bits[2:1] (see Figure 52 and Figure 53).

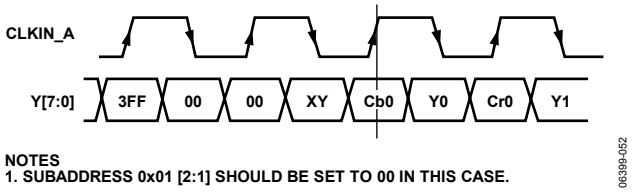


Figure 52. ED/HD-DDR Input Sequence (EAV/SAV)—Option A

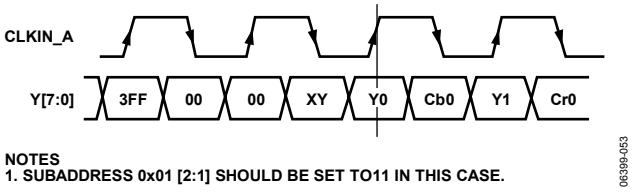


Figure 53. ED/HD-DDR Input Sequence (EAV/SAV)—Option B

24-Bit 4:4:4 YCrCb Mode

Subaddress 0x35, Bit 1 = 0; Subaddress 0x33, Bit 6 = 0

In 24-bit 4:4:4 YCrCb input mode, the Y pixel data is input on Pin Y7 to Pin Y0, with Y0 being the LSB.

The Cr pixel data is input on Pin S7 to Pin S0, with S0 being the LSB.

The Cb pixel data is input on Pin C7 to Pin C0, with C0 being the LSB.

24-Bit 4:4:4 RGB Mode

Subaddress 0x35, Bit 1 = 1

In 24-bit 4:4:4 RGB input mode, the red pixel data is input on Pin S7 to Pin S0, the green pixel data is input on Pin Y7 to Pin Y0, and the blue pixel data is input on Pin C7 to Pin C0. S0, Y0, and C0 are the respective bus LSBs.

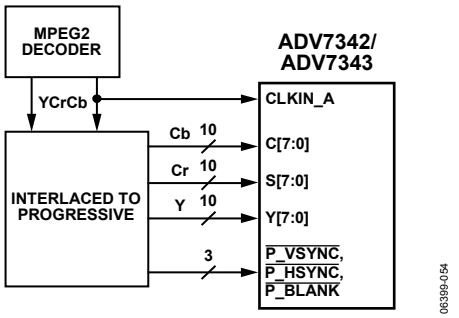


Figure 54. ED/HD Only Example Application

SIMULTANEOUS STANDARD DEFINITION AND ENHANCED DEFINITION/HIGH DEFINITION

Subaddress 0x01, Bits[6:4] = 011 or 100

The ADV7342/ADV7343 are able to simultaneously process SD 4:2:2 YCrCb data and ED/HD 4:2:2 YCrCb data. The 27 MHz SD clock signal must be provided on the CLKIN_A pin. The ED/HD clock signal must be provided on the CLKIN_B pin. SD input synchronization signals are provided on the S_HSYNC and S_VSYNC pins. ED/HD input synchronization signals are provided on the P_HSYNC, P_VSYNC and P_BLANK pins.

SD 8-Bit 4:2:2 YCrCb and ED/HD-SDR 16-Bit 4:2:2 YCrCb

The SD 8-bit 4:2:2 YCrCb pixel data is input on Pin S7 to Pin S0, with S0 being the LSB.

The ED/HD 16-bit 4:2:2 Y pixel data is input on Pin Y7 to Pin Y0, with Y0 being the LSB.

The ED/HD 16-bit 4:2:2 CrCb pixel data is input on Pin C7 to Pin C0, with C0 being the LSB.

SD 8-Bit 4:2:2 YCrCb and ED/HD-DDR 8-Bit 4:2:2 YCrCb

The SD 8-bit 4:2:2 YCrCb pixel data is input on Pin S7 to Pin S0, with S0 being the LSB.

The ED/HD-DDR 8-bit 4:2:2 Y pixel data is input on Pin Y7 to Pin Y0 upon the rising or falling edge of CLKIN_B. Y0 is the LSB.

The ED/HD-DDR 8-bit 4:2:2 CrCb pixel data is also input on Pin Y7 to Pin Y0 upon the opposite edge of CLKIN_B. Y0 is the LSB.

Whether the ED/HD Y data is clocked in upon the rising or falling edge of CLKIN_B is determined by Subaddress 0x01, Bits[2:1] (See the input sequence shown in Figure 52 and Figure 53).

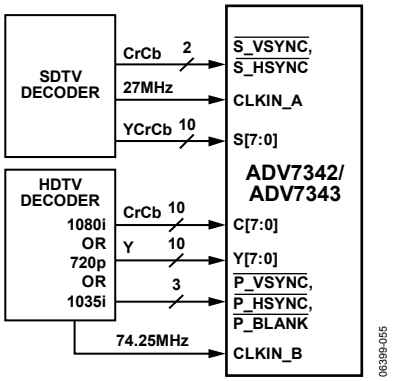


Figure 55. Simultaneous SD and ED Example Application

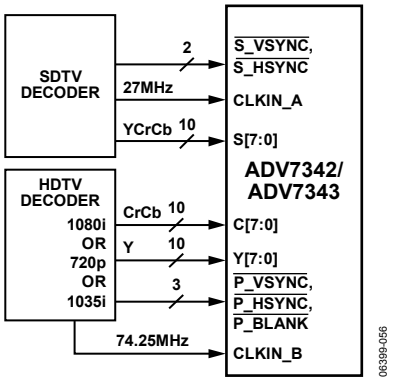


Figure 56. Simultaneous SD and HD Example Application

ENHANCED DEFINITION ONLY (AT 54 MHz)

Subaddress 0x01, Bits[6:4] = 111

Enhanced definition (ED) YCrCb data can be input in an interleaved 4:2:2 format on an 8-bit bus at a rate of 54 MHz.

A 54 MHz clock signal must be provided on the CLKIN_A pin. Input synchronization signals are provided on the $\overline{\text{P\_HSYNC}}$, $\overline{\text{P\_VSYNC}}$, and $\overline{\text{P\_BLANK}}$ pins.

The interleaved pixel data is input on Pin Y7 to Pin Y0, with Y0 being the LSB.

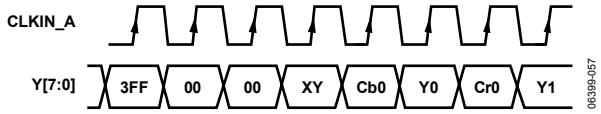


Figure 57. ED Only (at 54 MHz) Input Sequence (EAV/SAV)

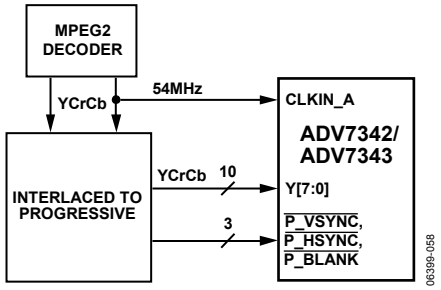


Figure 58. ED Only (at 54 MHz) Example Application

OUTPUT CONFIGURATION

The ADV7342/ADV7343 support a number of different output configurations. Table 32 to Table 35 lists all possible output configurations.

Table 32. SD Only Output Configurations

RGB/YPrPb Output Select[1] (0x02, Bit 5)	SD DAC Output 2 (0x82, Bit 2)	SD DAC Output 1 (0x82, Bit 1)	SD Luma/Chroma Swap (0x84, Bit 7)	DAC 1	DAC 2	DAC 3	DAC 4	DAC 5	DAC 6
0	0	0	0	G	B	R	CVBS	Luma	Chroma
0	0	0	1	G	B	R	CVBS	Chroma	Luma
0	0	1	0	CVBS	Luma	Chroma	G	B	R
0	0	1	1	CVBS	Chroma	Luma	G	B	R
0	1	0	0	CVBS	B	R	G	Luma	Chroma
0	1	0	1	CVBS	B	R	G	Chroma	Luma
0	1	1	0	G	Luma	Chroma	CVBS	B	R
0	1	1	1	G	Chroma	Luma	CVBS	B	R
1	0	0	0	Y	Pb	Pr	CVBS	Luma	Chroma
1	0	0	1	Y	Pb	Pr	CVBS	Chroma	Luma
1	0	1	0	CVBS	Luma	Chroma	Y	Pb	Pr
1	0	1	1	CVBS	Chroma	Luma	Y	Pb	Pr
1	1	0	0	CVBS	Pb	Pr	Y	Luma	Chroma
1	1	0	1	CVBS	Pb	Pr	Y	Chroma	Luma
1	1	1	0	Y	Luma	Chroma	CVBS	Pb	Pr
1	1	1	1	Y	Chroma	Luma	CVBS	Pb	Pr

[1] If SD RGB output is selected, a color reversal is possible using Subaddress 0x86, Bit 7.

Table 33. ED/HD Only Output Configurations

RGB/YPrPb Output Select (0x02, Bit 5)	ED/HD Color DAC Swap (0x35, Bit 3)	DAC 1	DAC 2	DAC 3	DAC 4	DAC 5	DAC 6
0	0	G	B	R	N/A	N/A	N/A
0	1	G	R	B	N/A	N/A	N/A
1	0	Y	Pb	Pr	N/A	N/A	N/A
1	1	Y	Pr	Pb	N/A	N/A	N/A

Table 34. Simultaneous SD and ED/HD Output Configurations

RGB/YPrPb Output Select (0x02, Bit 5)	ED/HD Color DAC Swap (0x35, Bit 3)	SD Luma/Chroma Swap (0x84, Bit 7)	DAC 1 (ED/HD)	DAC 2 (ED/HD)	DAC 3 (ED/HD)	DAC 4 (SD)	DAC 5 (SD)	DAC 6 (SD)
0	0	0	G	B	R	CVBS	Luma	Chroma
0	0	1	G	B	R	CVBS	Chroma	Luma
0	1	0	G	R	B	CVBS	Luma	Chroma
0	1	1	G	R	B	CVBS	Chroma	Luma
1	0	0	Y	Pb	Pr	CVBS	Luma	Chroma
1	0	1	Y	Pb	Pr	CVBS	Chroma	Luma
1	1	0	Y	Pr	Pb	CVBS	Luma	Chroma
1	1	1	Y	Pr	Pb	CVBS	Chroma	Luma

Table 35. ED Only (at 54 MHz) Output Configurations

RGB/YPrPb Output Select (0x02, Bit 5)	ED/HD Color DAC Swap (0x35, Bit 3)	DAC 1	DAC 2	DAC 3	DAC 4	DAC 5	DAC 6
0	0	G	B	R	N/A	N/A	N/A
0	1	G	R	B	N/A	N/A	N/A
1	0	Y	Pb	Pr	N/A	N/A	N/A
1	1	Y	Pr	Pb	N/A	N/A	N/A

FEATURES

OUTPUT OVERSAMPLING

The ADV7342/ADV7343 include two on-chip phase locked loops (PLLs) that allow for oversampling of SD, ED, and HD video data. Table 36 shows the various oversampling rates supported in the ADV7342/ADV7343.

SD Only, ED Only, and HD Only Modes

PLL 1 is used in SD only, ED only, and HD only modes. PLL 2 is unused in these modes. PLL 1 is disabled by default and can be enabled using Subaddress 0x00, Bit 1 = 0.

SD and ED/HD Simultaneous Modes

Both PLL 1 and PLL 2 are used in simultaneous modes. The use of two PLLs allows for independent oversampling of SD and ED/HD video. PLL 1 is used to oversample SD video data, and PLL 2 is used to oversample ED/HD video data. In simultaneous modes, PLL 2 is always enabled. PLL 1 is disabled by default and can be enabled using Subaddress 0x00, Bit 1 = 0.

ED/HD NONSTANDARD TIMING MODE

Subaddress 0x30, Bits[7:3] = 00001

For any ED/HD input data that does not conform to the standards available in the ED/HD input mode table (Subaddress 0x30, Bits[7:3]), the ED/HD nonstandard timing mode can be used to interface to the ADV7342/ADV7343.

ED/HD nonstandard timing mode can be enabled by setting Subaddress 0x30, Bits[7:3] to 00001.

A clock signal must be provided on the CLKIN_A pin. P_HSYNC and P_VSYNC must be toggled by the user to generate the appropriate horizontal and vertical synchronization pulses on the analog output from the encoder. Figure 59 illustrates the various output levels that can be generated .Table 37 lists the transitions required to generate these output levels.

Embedded EAV/SAV timing codes are not supported in ED/HD nonstandard timing mode.

The user must ensure that appropriate pixel data is applied to the encoder where the blanking level is expected at the output.

Macrovision (ADV7342 only) and output oversampling are not available in ED/HD nonstandard timing mode.

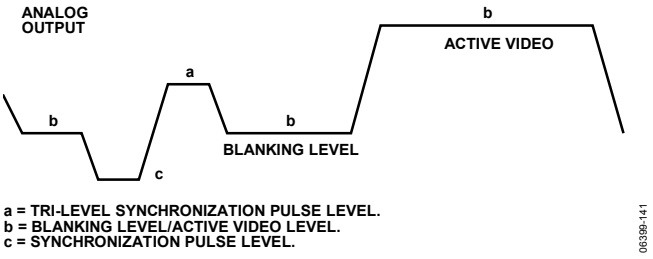


Figure 59. ED/HD Nonstandard Timing Mode Output Levels

Table 36. Output Oversampling Modes and Rates

Input Mode Subaddress 0x01 [6:4]		PLL and Oversampling Control Subaddress 0x00, Bit 1	Oversampling Mode and Rate
000	SD only	1	SD (2×)
000	SD only	0	SD (16×)
001/010	ED only	1	ED (1×)
001/010	ED only	0	ED (8×)
001/010	HD only	1	HD (1×)
001/010	HD only	0	HD (4×)
011/100	SD and ED	1	SD (2×) and ED (8×)
011/100	SD and ED	0	SD (16×) and ED (8×)
011/100	SD and HD	1	SD (2×) and HD (4×)
011/100	SD and HD	0	SD (16×) and HD (4×)
111	ED only (at 54 MHz)	1	ED only (at 54 MHz) (1×)
111	ED only (at 54 MHz)	0	ED only (at 54 MHz) (8×)

Table 37. ED/HD Nonstandard Timing Mode Synchronization Signal Generation

Output Level Transition[1]	$\overline{\text{P\_HSYNC}}$	$\overline{\text{P\_VSYNC}}$
b → c	1 → 0	1 → 0 or 0[2]
c → a	0	0 → 1
a → b	0 → 1	1
c → b	0 → 1	0

[1] a = tri-level synchronization pulse level; b = blanking level/active video level; c = synchronization pulse level.
[2] If $\overline{\text{P\_VSYNC}}$ = 1, it should transition to 0. If $\overline{\text{P\_VSYNC}}$ = 0, it should remain at 0. If tri-level synchronization pulse generation is not required, $\overline{\text{P\_VSYNC}}$ should always be 0.

ED/HD TIMING RESET

Subaddress 0x34, Bit 0

An ED/HD timing reset is achieved by toggling the ED/HD timing reset control bit (Subaddress 0x34, Bit 0) from 0 to 1. In this state, the horizontal and vertical counters remain reset. When this bit is set back to 0, the internal counters resume counting. This timing reset applies to the ED/HD timing counters only.

SD SUBCARRIER FREQUENCY LOCK, SUBCARRIER PHASE RESET, AND TIMING RESET

Subaddress 0x84, Bits[2:1]

Together with the SFL/MISO pin and SD Mode Register 4 (Subaddress 0x84, Bits[2:1]), the ADV7342/ADV7343 can be used in timing reset mode, subcarrier phase reset mode, or SFL mode.

Timing Reset (TR) Mode

In this mode (Subaddress 0x84, Bits[2:1] = 10), a timing reset is achieved in a low-to-high transition on the SFL/MISO pin (Pin 48). In this state, the horizontal and vertical counters remain reset.

Upon releasing this pin (set to low), the internal counters resume counting, starting with Field 1, and the subcarrier phase is reset.

The minimum time the pin must be held high is one clock cycle; otherwise, this reset signal might not be recognized. This timing reset applies to the SD timing counters only.

Subcarrier Phase Reset (SCR) Mode

In this mode (Subaddress 0x84, Bits[2:1] = 01), a low-to-high transition on the SFL/MISO pin (Pin 48) resets the subcarrier phase to 0 on the field following the subcarrier phase reset. This reset signal must be held high for a minimum of one clock cycle.

Because the field counter is not reset, it is recommended that the reset signal be applied in Field 7 (PAL) or Field 3 (NTSC). The reset of the phase then occurs on the next field, that is, Field 1, lined up correctly with the internal counters. The field count register at Subaddress 0xBB can be used to identify the number of the active field.

Subcarrier Frequency Lock (SFL) Mode

In this mode (Subaddress 0x84, Bits[2:1] = 11), the ADV7342 /ADV7343 can be used to lock to an external video source. The SFL mode allows the ADV7342/ADV7343 to automatically alter the subcarrier frequency to compensate for line length variations. When the part is connected to a device such as an ADV7403 video decoder (see Figure 62) that outputs a digital data stream in the SFL format, the part automatically changes to the compensated subcarrier frequency on a line-by-line basis. This digital data stream is 67 bits wide, and the subcarrier is contained in Bit 0 to Bit 21. Each bit is two clock cycles long.

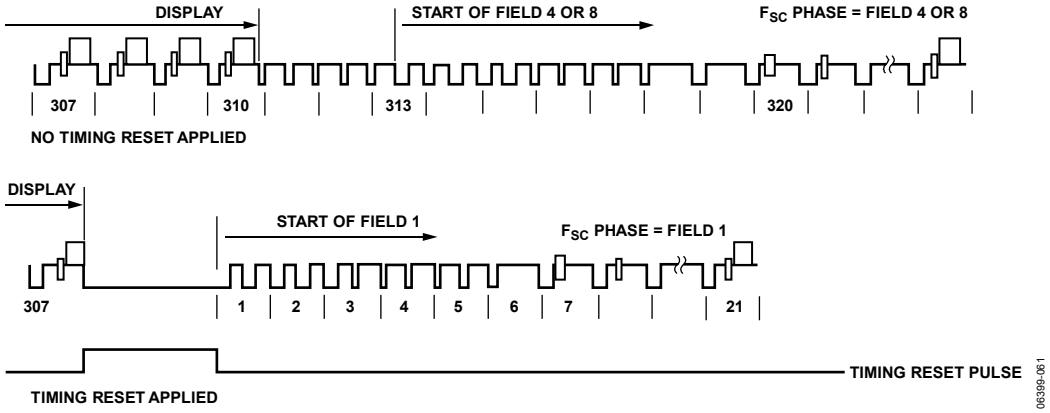


Figure 60. SD Timing Reset Timing Diagram (Subaddress 0x84, Bits [2:1] = 10)

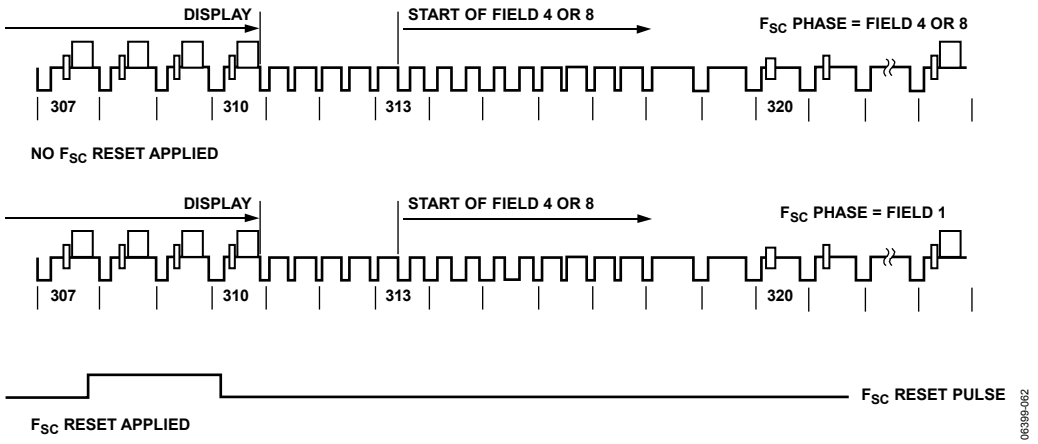


Figure 61. SD Subcarrier Phase Reset Timing Diagram (Subaddress 0x84, Bits [2:1] = 01)

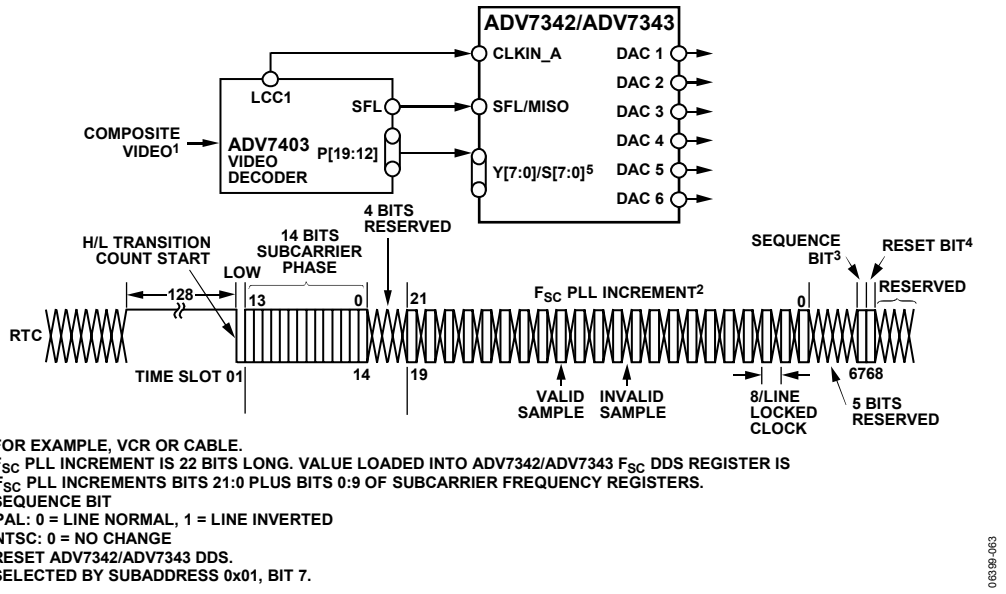


Figure 62. SD Subcarrier Frequency Lock Timing and Connections Diagram (Subaddress 0x84, Bits [2:1] = 11)

SD VCR FF/RW SYNC

Subaddress 0x82, Bit 5

In DVD record applications where the encoder is used with a decoder, the VCR FF/RW sync control bit can be used for non-standard input video, that is, in fast forward or rewind modes.

In fast forward mode, the sync information at the start of a new field in the incoming video usually occurs before the correct number of lines/fields is reached. In rewind mode, this sync signal usually occurs after the total number of lines/fields is reached. Conventionally, this means that the output video has corrupted field signals because one signal is generated by the incoming video and another is generated when the internal line/field counters reach the end of a field.

When the VCR FF/RW sync control is enabled (Subaddress 0x82, Bit 5), the line/field counters are updated according to the incoming $\overline{\text{VSYNC}}$ signal and when the analog output matches the incoming $\overline{\text{VSYNC}}$ signal.

This control is available in all slave-timing modes except Slave Mode 0.

VERTICAL BLANKING INTERVAL

Subaddress 0x31, Bit 4; Subaddress 0x83, Bit 4

The ADV7342/ADV7343 are able to accept input data that contains VBI data (such as CGMS, WSS, and VITS) in SD, ED, and HD modes.

If VBI is disabled (Subaddress 0x31, Bit 4 for ED/HD; Subaddress 0x83, Bit 4 for SD), VBI data is not present at the output and the entire VBI is blanked. These control bits are valid in all master and slave timing modes.

For the SMPTE 293M (525p) standard, VBI data can be inserted on Line 13 to Line 42 of each frame, or on Line 6 to Line 43 for the ITU-R BT.1358 (625p) standard.

VBI data can be present on Line 10 to Line 20 for NTSC and on Line 7 to Line 22 for PAL.

In SD Timing Mode 0 (slave option), if VBI is enabled, the blanking bit in the EAV/SAV code is overwritten. It is possible to use VBI in this timing mode as well.

If CGMS is enabled and VBI is disabled, the CGMS data is nevertheless available at the output.

SD SUBCARRIER FREQUENCY REGISTERS

Subaddress 0x8C to Subaddress 0x8F

Four 8-bit registers are used to set up the subcarrier frequency. The value of these registers is calculated using:

$$\textit{Subcarrier Frequency Register} = \frac{\textit{Number of subcarrier periods in one video line}}{\textit{Number of 27 MHz clk cycles in one video line}} \times 2^{32}$$

where the sum is rounded to the nearest integer.

For example, in NTSC mode:

$$\textit{Subcarrier Register Value} = \left(\frac{227.5}{1716}\right) \times 2^{32} = 569408543$$

where:

Subcarrier Register Value = 569408543d = 0×21F07C1F
SD F_{SC} Register 0: 0x1F
SD F_{SC} Register 1: 0x7C
SD F_{SC} Register 2: 0xF0
SD F_{SC} Register 3: 0x21

Programming the F_{SC}

The subcarrier frequency register value is divided into four F_{SC} registers as shown in the previous example. The four subcarrier frequency registers must be updated sequentially, starting with Subcarrier Frequency Register 0 and ending with Subcarrier Frequency Register 3. The subcarrier frequency updates only after the last subcarrier frequency register byte has been received by the ADV7342/ADV7343.

Typical F_{SC} Values

Table 38 outlines the values that should be written to the subcarrier frequency registers for NTSC and PAL B/D/G/H/I.

Table 38. Typical F_{SC} Values

Subaddress	Description	NTSC	PAL B/D/G/H/I
0x8C	$F_{SC}0$	0x1F	0xCB
0x8D	$F_{SC}1$	0x7C	0x8A
0x8E	$F_{SC}2$	0xF0	0x09
0x8F	$F_{SC}3$	0x21	0x2A

SD NONINTERLACED MODE

Subaddress 0x88, Bit 1

The ADV7342/ADV7343 support a SD noninterlaced mode. Using this mode, progressive inputs at twice the frame rate of NTSC and PAL (240p/59.94 Hz and 288p/50 Hz, respectively) can be input into the ADV7342/ADV7343. The SD noninterlaced mode can be enabled using Subaddress 0x88, Bit 1.

A 27 MHz clock signal must be provided on the CLKIN_A pin. Embedded EAV/SAV timing codes or external horizontal and vertical synchronization signals provided on the $\overline{\text{S\_HSYNC}}$ and $\overline{\text{S\_VSYNC}}$ pins can be used to synchronize the input pixel data.

All input configurations, output configurations and features available in NTSC and PAL modes are available in SD non-interlaced mode.

For 240p/59.94 Hz input, the ADV7342/ADV7343 should be configured for NTSC operation and Subaddress 0x88, Bit 1 should be set to 1.

For 288p/50 Hz input, the ADV7342/ADV7343 should be configured for PAL operation and Subaddress 0x88, Bit 1 should be set to 1.

SD SQUARE PIXEL MODE

Subaddress 0x82, Bit 4

The ADV7342/ADV7343 can be used to operate in square pixel mode (Subaddress 0x82, Bit 4). For NTSC operation, an input clock of 24.5454 MHz is required. Alternatively, for PAL operation, an input clock of 29.5 MHz is required.

The internal timing logic adjusts accordingly for square pixel mode operation. In square pixel mode, the timing diagrams shown in Figure 63 and Figure 64 apply.

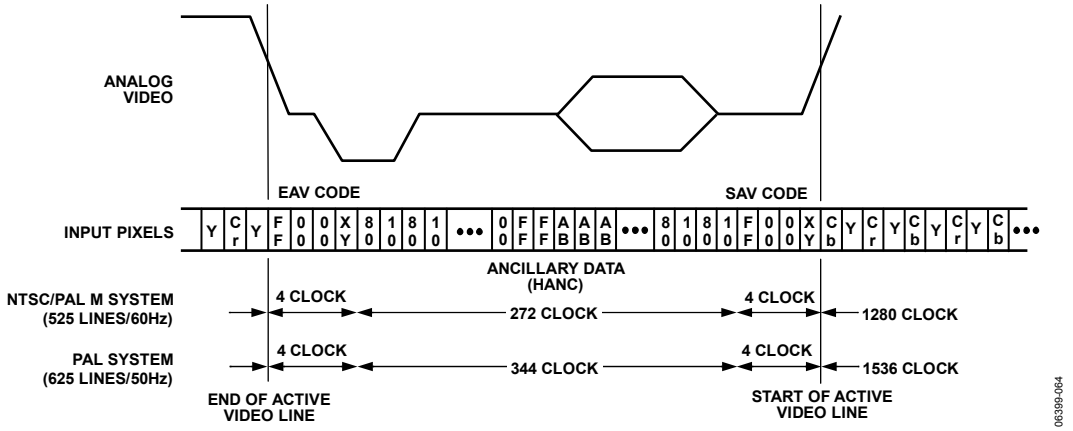


Figure 63. Square Pixel Mode EAV/SAV Embedded Timing

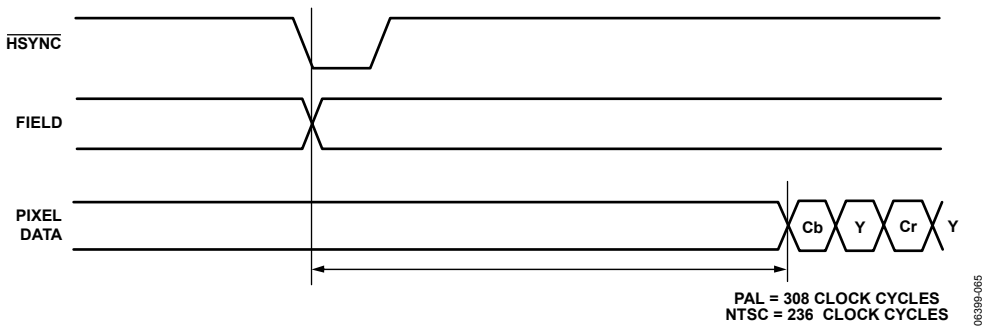


Figure 64. Square Pixel Mode Active Pixel Timing

FILTERS

Table 39 shows an overview of the programmable filters available on the ADV7342/ADV7343.

Table 39. Selectable Filters

Filter	Subaddress
SD Luma LPF NTSC	0x80
SD Luma LPF PAL	0x80
SD Luma Notch NTSC	0x80
SD Luma Notch PAL	0x80
SD Luma SSAF	0x80
SD Luma CIF	0x80
SD Luma QCIF	0x80
SD Chroma 0.65 MHz	0x80
SD Chroma 1.0 MHz	0x80
SD Chroma 1.3 MHz	0x80
SD Chroma 2.0 MHz	0x80
SD Chroma 3.0 MHz	0x80
SD Chroma CIF	0x80
SD Chroma QCIF	0x80
SD PrPb SSAF	0x82
ED/HD Chroma Input	0x33
ED/HD Sinc Compensation Filter	0x33
ED/HD Chroma SSAF	0x33

SD Internal Filter Response

Subaddress 0x80, Bits[7:2]; Subaddress 0x82, Bit 0

The Y filter supports several different frequency responses, including two low-pass responses, two notch responses, an extended (SSAF) response with or without gain boost attenuation, a CIF response, and a QCIF response. The PrPb filter supports several different frequency responses, including six low-pass responses, a CIF response, and a QCIF response, as shown in Figure 39 and Figure 40.

If SD SSAF gain is enabled (Subaddress 0x87, Bit 4), there are 13 response options in the −4 dB to +4 dB range. The desired response can be programmed using Subaddress 0xA2. The variation of frequency responses is shown in Figure 36 to Figure 38.

In addition to the chroma filters listed in Table 39, the ADV7342/ADV7343 contain an SSAF filter specifically designed for the color difference component outputs, Pr and Pb. This filter has a cutoff frequency of ~2.7 MHz and a gain of −40 dB at 3.8 MHz (see Figure 65). This filter can be controlled with Subaddress 0x82, Bit 0.

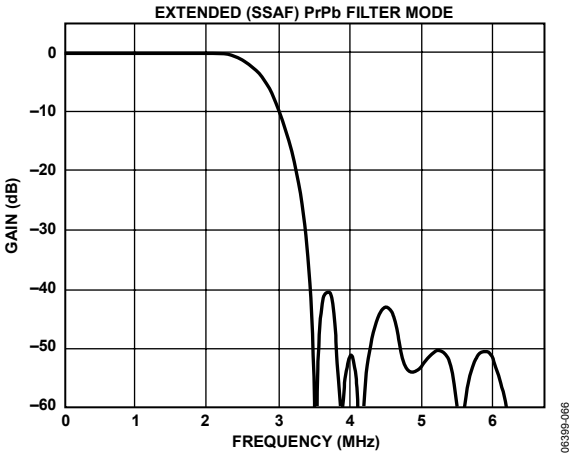


Figure 65. PrPb SSAF Filter

If this filter is disabled, one of the chroma filters shown in Table 40 can be selected and used for the CVBS or luma/chroma signal.

Table 40. Internal Filter Specifications

Filter	Pass-Band Ripple (dB)[1]	3 dB Bandwidth (MHz)[2]
Luma LPF NTSC	0.16	4.24
Luma LPF PAL	0.1	4.81
Luma Notch NTSC	0.09	2.3/4.9/6.6
Luma Notch PAL	0.1	3.1/5.6/6.4
Luma SSAF	0.04	6.45
Luma CIF	0.127	3.02
Luma QCIF	Monotonic	1.5
Chroma 0.65 MHz	Monotonic	0.65
Chroma 1.0 MHz	Monotonic	1
Chroma 1.3 MHz	0.09	1.395
Chroma 2.0 MHz	0.048	2.2
Chroma 3.0 MHz	Monotonic	3.2
Chroma CIF	Monotonic	0.65
Chroma QCIF	Monotonic	0.5

[1] Pass-band ripple is the maximum fluctuation from the 0 dB response in the pass band, measured in dB. The pass band is defined to have 0 Hz to fc (Hz) frequency limits for a low-pass filter, and 0 Hz to f1 (Hz) and f2 (Hz) to infinity for a notch filter, where fc, f1, and f2 are the −3 dB points.
[2] 3 dB bandwidth refers to the −3 dB cutoff frequency.

ED/HD Sinc Compensation Filter Response

Subaddress 0x33, Bit 3

The ADV7342/ADV7343 include a filter designed to counter the effect of sinc roll-off in DAC 1, DAC 2, and DAC 3 while operating in ED/HD mode. This filter is enabled by default. It can be disabled using Subaddress 0x33, Bit 3. The benefit of the filter is illustrated in Figure 66 and Figure 67.

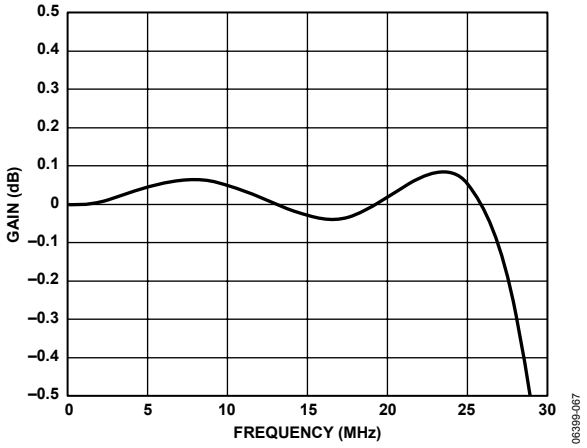


Figure 66. ED/HD Sinc Compensation Filter Enabled

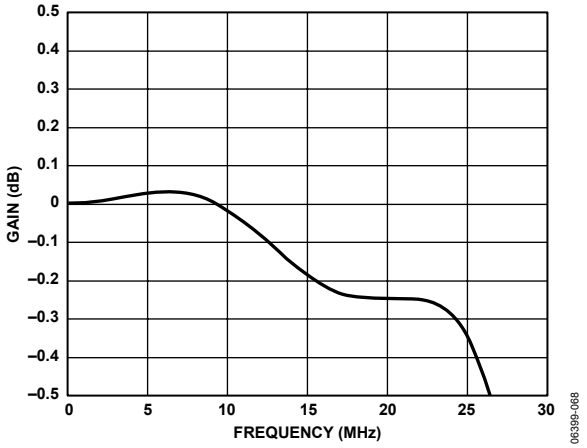


Figure 67. ED/HD Sinc Compensation Filter Disabled

ED/HD TEST PATTERN COLOR CONTROLS

Subaddress 0x36 to Subaddress 0x38

Three 8-bit registers at Subaddress 0x36 to Subaddress 0x38 are used to program the output color of the internal ED/HD test pattern generator (Subaddress 0x31, Bit 2 = 1), whether it be the lines of the cross hatch pattern or the uniform field test pattern. They are not functional as color controls for external pixel data input.

The values for the luma (Y) and the color difference (Cr and Cb) signals used to obtain white, black, and saturated primary and complementary colors conform to the ITU-R BT.601-4 standard.

Table 41 shows sample color values that can be programmed into the color registers when the output standard selection is set to EIA 770.2/EIA 770.3 (Subaddress 0x30, Bits[1:0] = 00).

Table 41. Sample Color Values for EIA 770.2/EIA 770.3 ED/HD Output Standard Selection

Sample Color	Y Value		Cr Value		Cb Value	
White	235	(0xEB)	128	(0x80)	128	(0x80)
Black	16	(0x10)	128	(0x80)	128	(0x80)
Red	81	(0x51)	240	(0xF0)	90	(0x5A)
Green	145	(0x91)	34	(0x22)	54	(0x36)
Blue	41	(0x29)	110	(0x6E)	240	(0xF0)
Yellow	210	(0xD2)	146	(0x92)	16	(0x10)
Cyan	170	(0xAA)	16	(0x10)	166	(0xA6)
Magenta	106	(0x6A)	222	(0xDE)	202	(0xCA)

COLOR SPACE CONVERSION MATRIX

Subaddress 0x03 to Subaddress 0x09

The internal color space conversion (CSC) matrix automatically performs all color space conversions based on the input mode programmed in the mode select register (Subaddress 0x01, Bits[6:4]). Table 42 and Table 43 show the options available in this matrix.

An SD color space conversion from RGB-in to YPrPb-out is possible. An ED/HD color space conversion from RGB-in to YPrPb-out is not possible.

Table 42. SD Color Space Conversion Options

Input	Output[1]	YPrPb/RGB Out (Reg. 0x02, Bit 5)	RGB In/YCrCb In (Reg. 0x87, Bit 7)
YCrCb	YPrPb	1	0
YCrCb	RGB	0	0
RGB	YPrPb	1	1
RGB	RGB	0	1

[1] CVBS/YC outputs are available for all CSC combinations.

Table 43. ED/HD Color Space Conversion Options

Input	Output	YPrPb/RGB Out (Reg. 0x02, Bit 5)	RGB In/YCrCb In (Reg. 0x35, Bit 1)
YCrCb	YPrPb	1	0
YCrCb	RGB	0	0
RGB	RGB	0	1

ED/HD Manual CSC Matrix Adjust Feature

The ED/HD manual CSC matrix adjust feature provides custom coefficient manipulation for color space conversions and is used in ED and HD modes only. The ED/HD manual CSC matrix adjust feature can be enabled using Subaddress 0x02, Bit 3.

Normally, there is no need to enable this feature because the CSC matrix automatically performs the color space conversion based on the input mode chosen (ED or HD) and the input and output color spaces selected (see Table 43). For this reason, the ED/HD manual CSC matrix adjust feature is disabled by default.

If RGB output is selected, the ED/HD CSC matrix scalar uses the following equations:

$$R = GY \times Y + RV \times Pr$$

$$G = GY \times Y - (GU \times Pb) - (GV \times Pr)$$

$$B = GY \times Y + BU \times Pb$$

Note that subtractions are implemented in hardware.

If YPrPb output is selected, the following equations are used:

$$Y = GY \times Y$$

$$Pr = RV \times Pr$$

$$Pb = BU \times Pb$$

where:

GY = Subaddress 0x05, Bits[7:0] and Subaddress 0x03, Bits[1:0].
GU = Subaddress 0x06, Bits[7:0] and Subaddress 0x04, Bits[7:6].
GV = Subaddress 0x07, Bits[7:0] and Subaddress 0x04, Bits[5:4].
BU = Subaddress 0x08, Bits[7:0] and Subaddress 0x04, Bits[3:2].
RV = Subaddress 0x09, Bits[7:0] and Subaddress 0x04, Bits[1:0].

Upon power-up, the CSC matrix is programmed with the default values shown in Table 44.

Table 44. ED/HD Manual CSC Matrix Default Values

Subaddress	Default
0x03	0x03
0x04	0xF0
0x05	0x4E
0x06	0x0E
0x07	0x24
0x08	0x92
0x09	0x7C

When the ED/HD manual CSC matrix adjust feature is enabled, the default coefficient values in Subaddress 0x03 to Subaddress 0x09 are correct for the HD color space only. The color components are converted according to the following 1080i and 720p standards (SMPTE 274M, SMPTE 296M):

$$R = Y + 1.575Pr$$

$$G = Y - 0.468Pr - 0.187Pb$$

$$B = Y + 1.855Pb$$

The conversion coefficients should be multiplied by 315 before being written to the ED/HD CSC matrix registers This is reflected in the default values for GY = 0x13B, GU = 0x03B, GV = 0x093, BU = 0x248, and RV = 0x1F0.

If the ED/HD manual CSC matrix adjust feature is enabled and another input standard (such as ED) is used, the scale values for GY, GU, GV, BU, and RV must be adjusted according to this input standard color space. The user should consider that the color component conversion could use different scale values.

For example, SMPTE 293M uses the following conversion:

$$R = Y + 1.402Pr$$

$$G = Y - 0.714Pr - 0.344Pb$$

$$B = Y + 1.773Pb$$

The programmable CSC matrix is used for external ED/HD pixel data and is not functional when internal test patterns are enabled.

Programming the CSC Matrix

If custom manipulation of the ED/HD CSC matrix coefficients is required for a YCrCb-to-RGB color space conversion, use the following procedure:

1. Enable the ED/HD manual CSC matrix adjust feature (Subaddress 0x02, Bit 3).
2. Set the output to RGB (Subaddress 0x02, Bit 5).
3. Disable sync on PrPb (Subaddress 0x35, Bit 2).
4. Enable sync on RGB (optional) (Subaddress 0x02, Bit 4).

The GY value controls the green signal output level, the BU value controls the blue signal output level, and the RV value controls the red signal output level.

SD LUMA AND COLOR CONTROL

Subaddress 0x9C to Subaddress 0x9F

SD Y Scale, SD Cb Scale, and SD Cr Scale are three 10-bit control registers that scale the SD Y, Cb, and Cr output levels.

Each of these registers represents the value required to scale the Cb or Cr level from 0.0 to 2.0 times its initial value and the Y level from 0.0 to 1.5 times its initial level. The value of these 10 bits is calculated using the following equation:

$$Y, Cb, or Cr\ Scale\ Value = Scale\ Factor \times 512$$

For example, if *Scale Factor* = 1.3

$$Y, Cb, or Cr\ Scale\ Value = 1.3 \times 512 = 665.6$$

Y, Cb, or Cr Scale Value = 666 *(rounded to the nearest integer)*

Y, Cb, or Cr Scale Value = 1010 0110 10b

Subaddress 0x9C, SD Scale LSB Register = 0x2A
Subaddress 0x9D, SD Y Scale Register = 0xA6
Subaddress 0x9E, SD Cb Scale Register = 0xA6
Subaddress 0x9F, SD Cr Scale Register = 0xA6

Note that this feature affects all interlaced output signals, that is, CVBS, Y/C, YPrPb, and RGB.

SD HUE ADJUST CONTROL

Subaddress 0xA0

When enabled, the SD hue adjust control register (Subaddress 0xA0) is used to adjust the hue on the SD composite and chroma outputs. This feature can be enabled using Subaddress 0x87, Bit 2.

Subaddress 0xA0 contains the bits required to vary the hue of the video data, that is, the variance in phase of the subcarrier during active video with respect to the phase of the subcarrier during the color burst. The ADV7342/ADV7343 provide a range of ±22.5° in increments of 0.17578125°. For normal operation (zero adjustment), this register is set to 0x80. Values 0xFF and 0x00 represent the upper and lower limits, respectively, of the attainable adjustment in NTSC mode. Values 0xFF and 0x01 represent the upper and lower limits, respectively, of the attainable adjustment in PAL mode.

The hue adjust value is calculated using the following equation:

$$Hue\ Adjust\ (°) = 0.17578125° \times (HCR_d - 128)$$

where HCR_d is the hue adjust control register (decimal)

For example, to adjust the hue by +4°, write 0x97 to the hue adjust control register.

$$\left(\frac{4}{0.17578125}\right) + 128 \approx 151d = 0x97$$

where the sum is rounded to the nearest integer.

To adjust the hue by −4°, write 0x69 to the hue adjust control register.

$$\left(\frac{-4}{0.17578125}\right) + 128 \approx 105d = 0x69$$

where the sum is rounded to the nearest integer.

SD BRIGHTNESS DETECT

Subaddress 0xBA

The ADV7342/ADV7343 allow monitoring of the brightness level of the incoming video data. The SD brightness detect register (Subaddress 0xBA) is a read-only register.

SD BRIGHTNESS CONTROL

Subaddress 0xA1, Bits[6:0]

When this feature is enabled, the SD brightness/WSS control register (Subaddress 0xA1) is used to control brightness by adding a programmable setup level onto the scaled Y data. This feature can be enabled using Subaddress 0x87, Bit 3.

For NTSC with pedestal, the setup can vary from 0 IRE to 22.5 IRE. For NTSC without pedestal and for PAL, the setup can vary from −7.5 IRE to +15 IRE.

The SD brightness control register is an 8-bit register. The seven LSBs of this 8-bit register are used to control the brightness level, which can be a positive or negative value.

For example, to add +20 IRE brightness level to an NTSC signal with pedestal, write 0x28 to Subaddress 0xA1.

$0 \times$ *(SD Brightness Value)* =

$0 \times$ (*IRE Value* $\times$ 2.015631) =

$0 \times (20 \times 2.015631) = 0 \times (40.31262) \approx 0x28$

To add −7 IRE brightness level to a PAL signal, write 0x72 to Subaddress 0xA1.

$0 \times$ (*SD Brightness Value*) =

$0 \times$ (*IRE Value* $\times$ 2.075631) =

$0 \times (7 \times 2.015631) = 0x(14.109417) \approx 0001110b$

0001110b *into twos complement* = 1110010b = 0x72

Table 45. Sample Brightness Control Values[1]

Setup Level (NTSC) with Pedestal	Setup Level (NTSC) Without Pedestal	Setup Level (PAL)	Brightness Control Value
22.5 IRE	15 IRE	15 IRE	0x1E
15 IRE	7.5 IRE	7.5 IRE	0x0F
7.5 IRE	0 IRE	0 IRE	0x00
0 IRE	−7.5 IRE	−7.5 IRE	0x71

[1] Values in the range of 0x3F to 0x44 could result in an invalid output signal.

SD INPUT STANDARD AUTO DETECTION

Subaddress 0x87, Bit 5

The ADV7342/ADV7343 include an SD input standard auto-detect feature. This SD feature can be enabled by setting Subaddress 0x87, Bit 5 to 1.

When enabled, the ADV7342/ADV7343 can automatically identify an NTSC or PAL B/D/G/H/I input stream. The ADV7342/ADV7343 automatically update the subcarrier frequency registers with the appropriate value for the identified standard. The ADV7342/ADV7343 are also configured to correctly encode the identified standard.

The SD standard bits (Subaddress 0x80, Bits[1:0]) and the subcarrier frequency registers are not updated to reflect the identified standard. All registers retain their default or user-defined values.

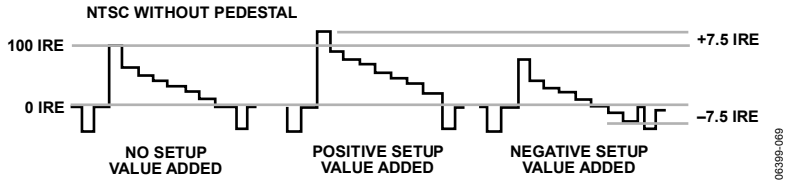


Figure 68. Examples of Brightness Control Values

DOUBLE BUFFERING

Subaddress 0x33, Bit 7 for ED/HD, Subaddress 0x88, Bit 2 for SD

Double-buffered registers are updated once per field. Double buffering improves overall performance, because modifications to register settings are not made during active video, but take effect prior to the start of the active video on the next field.

Double buffering can be activated on the following ED/HD registers using Subaddress 0x33, Bit 7: ED/HD Gamma A and Gamma B curves, and ED/HD CGMS registers.

Double buffering can be activated on the following SD registers using Subaddress 0x88, Bit 2: SD Gamma A and Gamma B curves, SD Y scale, SD Cr scale, SD Cb scale, SD brightness, SD closed captioning, and SD Macrovision Bits[5:0] (Subaddress 0xE0, Bits[5:0]).

PROGRAMMABLE DAC GAIN CONTROL

Subaddress 0x0A to Subaddress 0x0B

It is possible to adjust the DAC output signal gain up or down from its absolute level. This is illustrated in Figure 69.

DAC 4 to DAC 6 are controlled by Register 0x0A.

DAC 1 to DAC 3 are controlled by Register 0x0B.

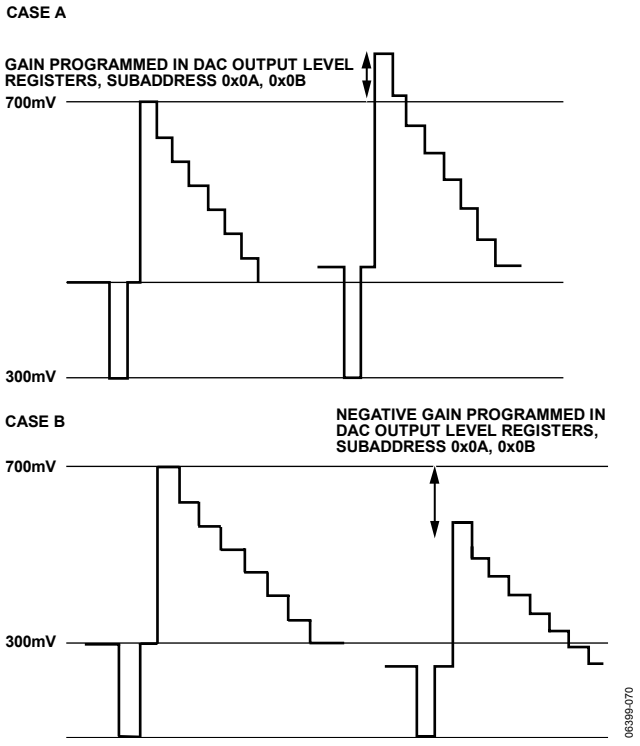


Figure 69. Programmable DAC Gain—Positive and Negative Gain

In Case A of Figure 69, the video output signal is gained. The absolute level of the sync tip and blanking level both increase with respect to the reference video output signal. The overall gain of the signal is increased from the reference signal.

In Case B of Figure 69, the video output signal is reduced. The absolute level of the sync tip and blanking level both decrease with respect to the reference video output signal. The overall gain of the signal is reduced from the reference signal.

The range of this feature is specified for ±7.5% of the nominal output from the DACs. For example, if the output current of the DAC is 4.33 mA, the DAC gain control feature can change this output current from 4.008 mA (−7.5%) to 4.658 mA (+7.5%).

The reset value of the control registers is 0x00, that is, nominal DAC current is output. Table 46 is an example of how the output current of the DACs varies for a nominal 4.33 mA output current.

Table 46. DAC Gain Control

Reg. 0x0A or Reg.0x0B	DAC Current (mA)	% Gain	Note
0100 0000 (0x40)	4.658	7.5000%	
0011 1111 (0x3F)	4.653	7.3820%	
0011 1110 (0x3E)	4.648	7.3640%	
...	...	...	
...	...	...	
0000 0010 (0x02)	4.43	0.0360%	
0000 0001 (0x01)	4.38	0.0180%	
0000 0000 (0x00)	4.33	0.0000%	Reset value, nominal
1111 1111 (0xFF)	4.25	−0.0180%	
1111 1110 (0xFE)	4.23	−0.0360%	
...	...	...	
...	...	...	
1100 0010 (0xC2)	4.018	−7.3640%	
1100 0001 (0xC1)	4.013	−7.3820%	
1100 0000 (0xC0)	4.008	−7.5000%	

GAMMA CORRECTION

Subaddress 0x44 to Subaddress 0x57 for ED/HD, Subaddress 0xA6 to Subaddress 0xB9 for SD

Generally, gamma correction is applied to compensate for the nonlinear relationship between signal input and output brightness level (as perceived on a CRT). It can also be applied wherever nonlinear processing is used.

Gamma correction uses the function

$$Signal_{OUT} = (Signal_{IN})^{\gamma}$$

where γ = is the gamma correction factor.

Gamma correction is available for SD and ED/HD video. For both variations, there are 20, 8-bit registers. They are used to program the Gamma Correction Curve A and Gamma Correction Curve B.

ED/HD gamma correction is enabled using Subaddress 0x35, Bit 5. ED/HD Gamma Correction Curve A is programmed at Subaddress 0x44 to Subaddress 0x4D, and ED/HD Gamma Correction Curve B is programmed at Subaddress 0x4E to Subaddress 0x57.

SD gamma correction is enabled using Subaddress 0x88, Bit 6. SD Gamma Correction Curve A is programmed at Subaddress 0xA6 to Subaddress 0xAF, and SD Gamma Correction Curve B is programmed at Subaddress 0xB0 to Subaddress 0xB9.

Gamma correction is performed on the luma data only. The user can choose one of two correction curves, Curve A or Curve B. Only one of these curves can be used at a time. For ED/HD gamma correction, curve selection is controlled using Subaddress 0x35, Bit 4. For SD gamma correction, curve selection is controlled using Subaddress 0x88, Bit 7.

The shape of the gamma correction curve is controlled by defining the curve response at 10 different locations along the curve. By altering the response at these locations, the shape of the gamma correction curve can be modified. Between these points, linear interpolation is used to generate intermediate values. Considering the curve has a total length of 256 points, the 10 programmable locations are at points 24, 32, 48, 64, 80, 96, 128, 160, 192, and 224. Locations 0, 16, 240, and 255 are fixed and cannot be changed.

From curve locations 16 to 240, the values at the programmable locations and, therefore, the response of the gamma correction curve should be calculated to produce the following result:

$$x_{DESIRED} = (x_{INPUT})^{\gamma}$$

where:
$x_{DESIRED}$ is the desired gamma corrected output.
x_{INPUT} is the linear input signal.
γ is the gamma correction factor.

To program the gamma correction registers, calculate the 10 programmable curve values using the following formula:

$$\gamma_n = \left(\left(\frac{n-16}{240-16} \right)^{\gamma} \times (240-16) \right) + 16$$

where:
γ_n is the value to be written into the gamma correction register for point n on the gamma correction curve.
n = 24, 32, 48, 64, 80, 96, 128, 160, 192, or 224.
γ is the gamma correction factor.

For example, setting γ = 0.5 for all programmable curve data points results in the following y_n values:

$y_{24} = [(8/224)^{0.5} \times 224] + 16 = 58$

$y_{32} = [(16/224)^{0.5} \times 224] + 16 = 76$

$y_{48} = [(32/224)^{0.5} \times 224] + 16 = 101$

$y_{64} = [(48/224)^{0.5} \times 224] + 16 = 120$

$y_{80} = [(64/224)^{0.5} \times 224] + 16 = 136$

$y_{96} = [(80/224)^{0.5} \times 224] + 16 = 150$

$y_{128} = [(112/224)^{0.5} \times 224] + 16 = 174$

$y_{160} = [(144/224)^{0.5} \times 224] + 16 = 195$

$y_{192} = [(176/224)^{0.5} \times 224] + 16 = 214$

$y_{224} = [(208/224)^{0.5} \times 224] + 16 = 232$

where the sum of each equation is rounded to the nearest integer.

The gamma curves in Figure 70 and Figure 71 are examples only; any user-defined curve in the range from 16 to 240 is acceptable.

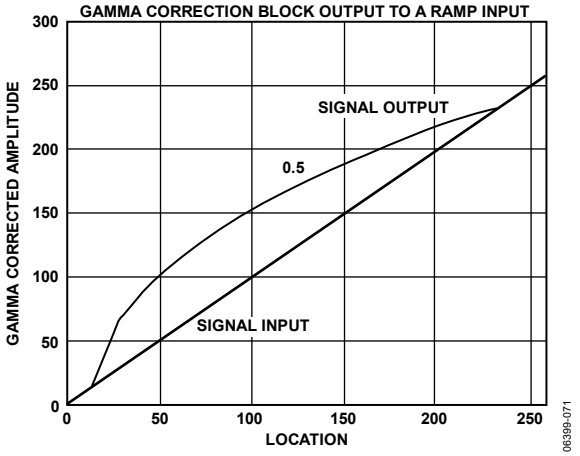


Figure 70. Signal Input (Ramp) and Signal Output for Gamma 0.5

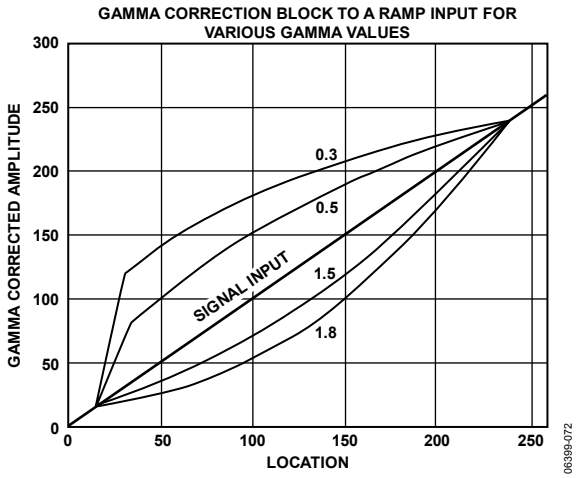


Figure 71. Signal Input (Ramp) and Selectable Output Curves

ED/HD SHARPNESS FILTER AND ADAPTIVE FILTER CONTROLS

Subaddress 0x40, Subaddress 0x58 to Subaddress 0x5D

There are three filter modes available on the ADV7342/ADV7343: a sharpness filter mode and two adaptive filter modes.

ED/HD Sharpness Filter Mode

To enhance or attenuate the Y signal in the frequency ranges shown in Figure 72, the ED/HD sharpness filter must be enabled (Subaddress 0x31, Bit 7) and the ED/HD adaptive filter must be disabled (Subaddress 0x35, Bit 7).

To select one of the 256 individual responses, the corresponding gain values, which range from –8 to +7 for each filter, must be programmed into the ED/HD sharpness filter gain register at Subaddress 0x40.

ED/HD Adaptive Filter Mode

The ED/HD Adaptive Filter Threshold A, B, and C registers, the ED/HD Adaptive Filter Gain 1, 2, and 3 registers, and the ED/HD sharpness filter gain register are used in adaptive filter mode. To activate the adaptive filter control, the ED/HD sharpness filter and the ED/HD adaptive filter must be enabled (Subaddress 0x31, Bit 7, and Subaddress 0x35, Bit 7, respectively).

The derivative of the incoming signal is compared to the three programmable threshold values: ED/HD Adaptive Filter Threshold A, B, and C (Subaddress 0x5B, Subaddress 0x5C, and Subaddress 0x5D, respectively). The recommended threshold range is 16 to 235, although any value in the range of 0 to 255 can be used.

The edges can then be attenuated with the settings in the ED/HD Adaptive Filter Gain 1, 2, and 3 registers (Subaddress 0x58, Subaddress 0x59, and Subaddress 0x5A, respectively), and the ED/HD sharpness filter gain register (Subaddress 0x40).

There are two adaptive filter modes available. The mode is selected using the ED/HD adaptive filter mode control (Subaddress 0x35, Bit 6):

- Mode A is used when the ED/HD adaptive filter mode control is set to 0. In this case, Filter B (LPF) is used in the adaptive filter block. In addition, only the programmed values for Gain B in the ED/HD sharpness filter gain register and ED/HD Adaptive Filter Gain 1, 2, and 3 registers are applied when needed. The Gain A values are fixed and cannot be changed.
- Mode B is used when ED/HD adaptive filter mode control is set to 1. In this mode, a cascade of Filter A and Filter B is used. Both settings for Gain A and Gain B in the ED/HD sharpness filter gain register and ED/HD Adaptive Filter Gain 1, 2, and 3 registers become active when needed.

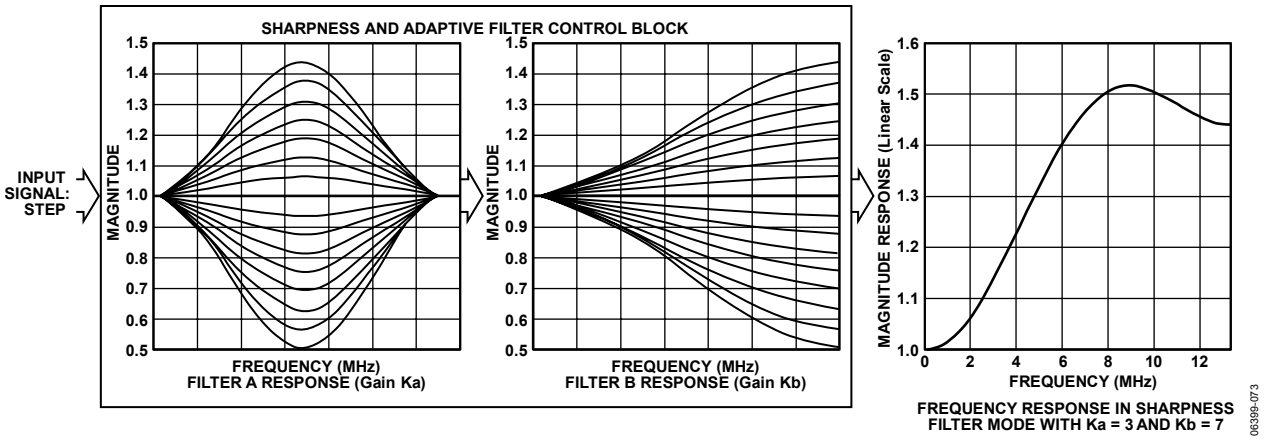


Figure 72. ED/HD Sharpness and Adaptive Filter Control Block

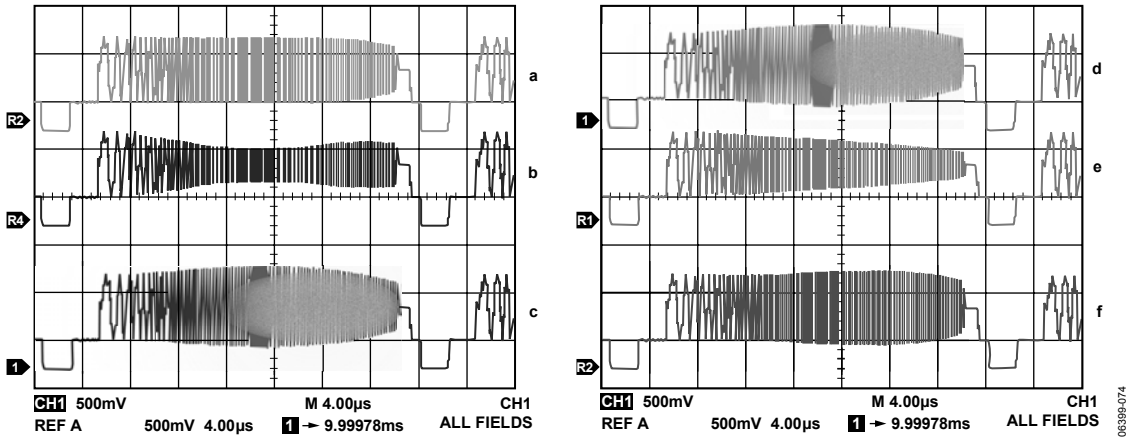


Figure 73. ED/ HD Sharpness Filter Control with Different Gain Settings for ED/HD Sharpness Filter Gain Values

ED/HD SHARPNESS FILTER AND ADAPTIVE FILTER APPLICATION EXAMPLES

Sharpness Filter Application

The ED/HD sharpness filter can be used to enhance or attenuate the Y video output signal. The register settings in Table 47 were used to achieve the results shown in Figure 73. Input data was generated by an external signal source.

Table 47. ED/HD Sharpness Control

Subaddress	Register Setting	Reference[1]
0x00	0xFC	
0x01	0x10	
0x02	0x20	
0x30	0x00	
0x31	0x81	
0x40	0x00	a
0x40	0x08	b
0x40	0x04	c
0x40	0x40	d
0x40	0x80	e
0x40	0x22	f

[1] See Figure 73.

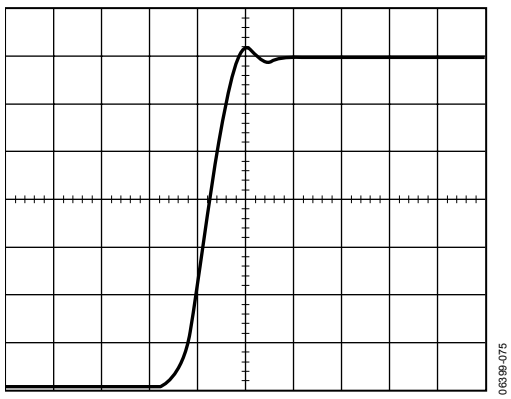


Figure 74. Input Signal to ED/HD Adaptive Filter

Adaptive Filter Control Application

The register settings in Table 48 are used to obtain the results shown in Figure 75, that is, to remove the ringing on the input Y signal, as shown in Figure 74. Input data is generated by an external signal source.

Table 48. Register Settings for Figure 75

Subaddress	Register Setting
0x00	0xFC
0x01	0x38
0x02	0x20
0x30	0x00
0x31	0x81
0x35	0x80
0x40	0x00
0x58	0xAC
0x59	0x9A
0x5A	0x88
0x5B	0x28
0x5C	0x3F
0x5D	0x64

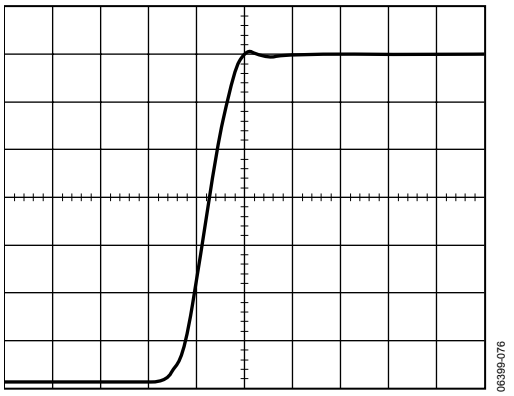


Figure 75. Output Signal from ED/HD Adaptive Filter (Mode A)

When changing the adaptive filter mode to Mode B (Subaddress 0x35, Bit 6), the output shown in Figure 76 can be obtained.

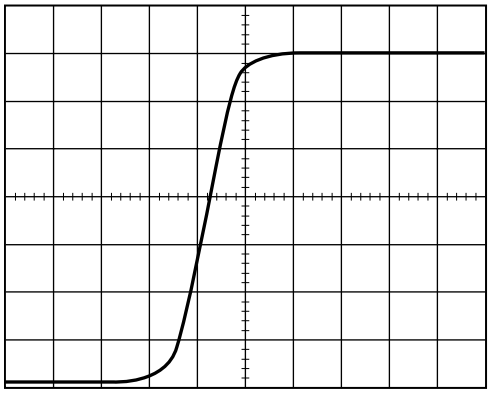


Figure 76. Output Signal from ED/HD Adaptive Filter (Mode B)

SD DIGITAL NOISE REDUCTION

Subaddress 0xA3 to Subaddress 0xA5

Digital noise reduction (DNR) is applied to the Y data only. A filter block selects the high frequency, low amplitude components of the incoming signal (DNR input select). The absolute value of the filter output is compared to a programmable threshold value (DNR threshold control). There are two DNR modes available, DNR mode and DNR sharpness mode.

In DNR mode, if the absolute value of the filter output is smaller than the threshold, it is assumed to be noise. A programmable amount (coring gain border, coring gain data) of this noise signal is subtracted from the original signal. In DNR sharpness mode, if the absolute value of the filter output is less than the programmed threshold, it is assumed to be noise. Otherwise, if the level exceeds the threshold, now identified as a valid signal, a fraction of the signal (coring gain border, coring gain data) is added to the original signal to boost high frequency components and sharpen the video image.

In MPEG systems, it is common to process the video information in blocks of 8 pixels × 8 pixels for MPEG2 systems, or 16 pixels × 16 pixels for MPEG1 systems (block size control). DNR can be applied to the resulting block transition areas that are known to contain noise. Generally, the block transition area contains two pixels. It is possible to define this area to contain four pixels (border area).

It is also possible to compensate for variable block positioning or differences in YCrCb pixel timing with the use of the DNR block offset.

The digital noise reduction registers are three 8-bit registers. They are used to control the DNR processing.

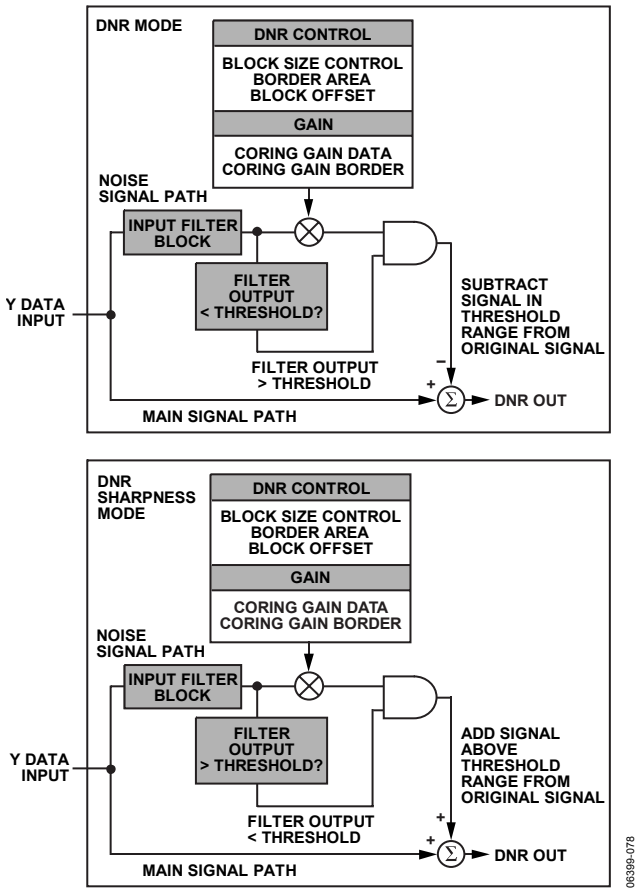


Figure 77. SD DNR Block Diagram

Coring Gain Border—Subaddress 0xA3, Bits[3:0]

These four bits are assigned to the gain factor applied to border areas. In DNR mode, the range of gain values is 0 to 1 in increments of 1/8. This factor is applied to the DNR filter output that lies below the set threshold range. The result is then subtracted from the original signal.

In DNR sharpness mode, the range of gain values is 0 to 0.5 in increments of 1/16. This factor is applied to the DNR filter output that lies above the threshold range. The result is added to the original signal.

Coring Gain Data—Subaddress 0xA3, Bits[7:4]

These four bits are assigned to the gain factor applied to the luma data inside the MPEG pixel block. In DNR mode, the range of gain values is 0 to 1 in increments of 1/8. This factor is applied to the DNR filter output that lies below the set threshold range. The result is then subtracted from the original signal.

In DNR sharpness mode, the range of gain values is 0 to 0.5 in increments of 1/16. This factor is applied to the DNR filter output that lies above the threshold range. The result is added to the original signal.

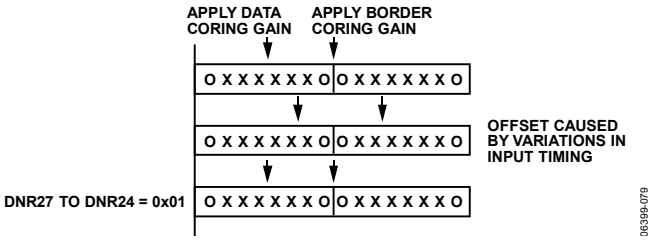


Figure 78. SD DNR Offset Control

DNR Threshold—Subaddress 0xA4, Bits[5:0]

These six bits are used to define the threshold value in the range of 0 to 63. The range is an absolute value.

Border Area—Subaddress 0xA4, Bit 6

When this bit is set to Logic 1, the block transition area can be defined to consist of four pixels. If this bit is set to Logic 0, the border transition area consists of two pixels, where one pixel refers to two clock cycles at 27 MHz.

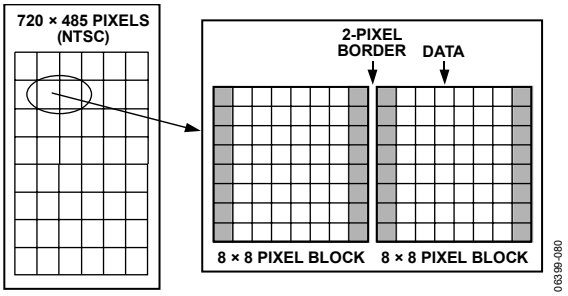


Figure 79. SD DNR Border Area

Block Size Control—Subaddress 0xA4, Bit 7

This bit is used to select the size of the data blocks to be processed. Setting the block size control function to Logic 1 defines a 16 pixel × 16 pixel data block, and Logic 0 defines an 8 pixel × 8 pixel data block, where one pixel refers to two clock cycles at 27 MHz.

DNR Input Select Control—Subaddress 0xA5, Bits[2:0]

Three bits are assigned to select the filter, which is applied to the incoming Y data. The signal that lies in the pass band of the selected filter is the signal that is DNR processed. Figure 80 shows the filter responses selectable with this control.

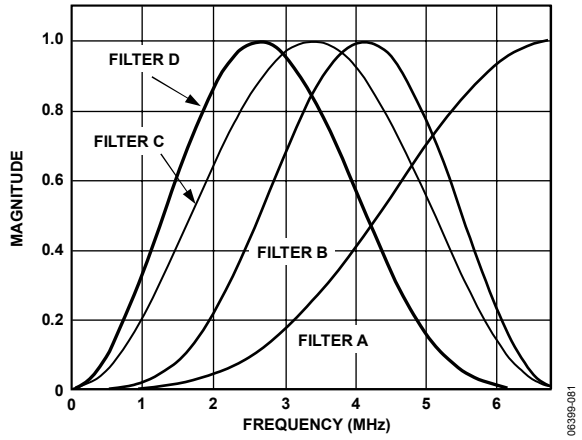


Figure 80. SD DNR Input Select

DNR Mode Control—Subaddress 0xA5, Bit 4

This bit controls the DNR mode selected. Logic 0 selects DNR mode; Logic 1 selects DNR sharpness mode.

DNR works on the principle of defining low amplitude, high frequency signals as probable noise and subtracting this noise from the original signal.

In DNR mode, it is possible to subtract a fraction of the signal that lies below the set threshold, assumed to be noise, from the original signal. The threshold is set in DNR Register 1.

When DNR sharpness mode is enabled, it is possible to add a fraction of the signal that lies above the set threshold to the original signal, because this data is assumed to be valid data and not noise. The overall effect is that the signal is boosted (similar to using the extended SSAF filter).

DNR Block Offset Control—Subaddress 0xA5, Bits[7:4]

Four bits are assigned to this control, which allows a shift of the data block of 15 pixels maximum. Consider the coring gain positions fixed. The block offset shifts the data in steps of one pixel such that the border coring gain factors can be applied at the same position regardless of variations in input timing of the data.

SD ACTIVE VIDEO EDGE CONTROL

Subaddress 0x82, Bit 7

The ADV7342/ADV7343 are able to control fast rising and falling signals at the start and end of active video in order to minimize ringing.

When the active video edge control feature is enabled (Subaddress 0x82, Bit 7 = 1), the first three pixels and the last three pixels of the active video on the luma channel are scaled so that maximum transitions on these pixels are not possible.

At the start of active video, the first three pixels are multiplied by 1/8, 1/2, and 7/8, respectively. Approaching the end of active video, the last three pixels are multiplied by 7/8, 1/2, and 1/8, respectively. All other active video pixels pass through unprocessed.

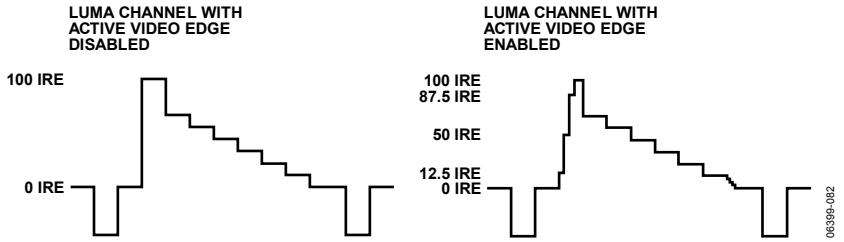


Figure 81. Example of Active Video Edge Functionality

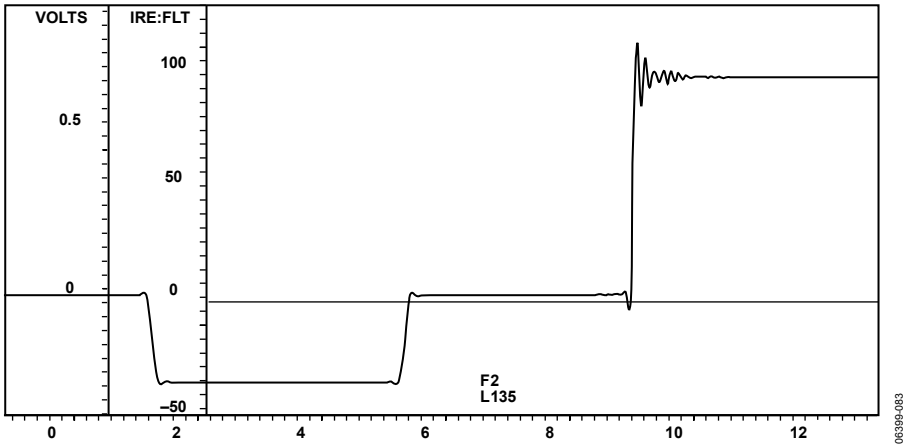


Figure 82. Example of Video Output with Subaddress 0x82, Bit 7 = 0

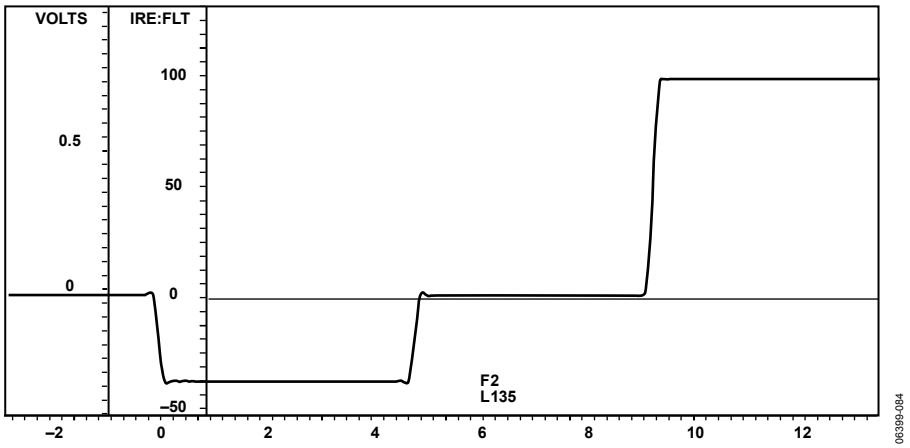


Figure 83. Example of Video Output with Subaddress 0x82, Bit 7 = 1

EXTERNAL HORIZONTAL AND VERTICAL SYNCHRONIZATION CONTROL

For timing synchronization purposes, the ADV7342/ADV7343 are able to accept either EAV/SAV time codes embedded in the input pixel data or external synchronization signals provided on the S_HSYNC, S_VSYNC, P_HSYNC, P_VSYNC, and P_BLANK pins (see Table 49). It is also possible to output synchronization signals on the S_HSYNC and S_VSYNC pins (see Table 50 to Table 52).

Table 49. Timing Synchronization Signal Input Options

Signal	Pin	Condition
SD HSYNC In	S_HSYNC	SD Slave Timing Mode 1, 2, or 3 Selected (Subaddress 0x8A[2:0]).[1]
SD VSYNC/FIELD In	S_VSYNC	SD Slave Timing Mode 1, 2, or 3 Selected (Subaddress 0x8A[2:0]).[1]
ED/HD HSYNC In	P_HSYNC	ED/HD Timing Synchronization Inputs Enabled (Subaddress 0x30, Bit 2 = 0).
ED/HD VSYNC/FIELD In	P_VSYNC	ED/HD Timing Synchronization Inputs Enabled (Subaddress 0x30, Bit 2 = 0).
ED/HD BLANK In	P_BLANK	

[1] SD and ED/HD timing synchronization outputs must also be disabled (Subaddress 0x02[7:6] = 00).

Table 50. Timing Synchronization Signal Output Options

Signal	Pin	Condition
SD HSYNC Out	S_HSYNC	SD Timing Synchronization Outputs Enabled (Subaddress 0x02, Bit 6 = 1).[1]
SD VSYNC/FIELD Out	S_VSYNC	SD Timing Synchronization Outputs Enabled (Subaddress 0x02, Bit 6 = 1).[1]
ED/HD HSYNC Out	S_HSYNC	ED/HD Timing Synchronization Outputs Enabled (Subaddress 0x02, Bit 7 = 1).
ED/HD VSYNC/FIELD Out	S_VSYNC	ED/HD Timing Synchronization Outputs Enabled (Subaddress 0x02, Bit 7 = 1).

[1] ED/HD timing synchronization outputs must also be disabled (Subaddress 0x02, Bit 7 = 0).

Table 51. S_HSYNC Output Control[1]

ED/HD Input Sync Format (0x30, Bit 2)	ED/HD HSYNC Control (0x34, Bit 1)	ED/HD Sync Output Enable (0x02, Bit 7)	SD Sync Output Enable (0x02, Bit 6)	Signal on S_HSYNC Pin	Duration
x	x	0	0	Tristate.	–
x	x	0	1	Pipelined SD HSYNC.	See Appendix 5—SD Timing.
0	0	1	x	Pipelined ED/HD HSYNC.	As per HSYNC timing.
1	0	1	x	Pipelined ED/HD HSYNC based on AV Code H bit.	Same as line blanking interval.
x	1	1	x	Pipelined ED/HD HSYNC based on horizontal counter.	Same as embedded HSYNC.

[1] In all ED/HD standards where there is an HSYNC output, the start of the HSYNC pulse is aligned with the falling edge of the embedded HSYNC in the output video.

Table 52. S_VSYNC Output Control[1]

ED/HD Input Sync Format (0x30, Bit 2)	ED/HD VSYNC Control (0x34, Bit 2)	ED/HD Sync Output Enable (0x02, Bit 7)	SD Sync Output Enable (0x02, Bit 6)	Video Standard	Signal on S_VSYNC Pin	Duration
x	X	0	0	x	Tristate.	–
x	X	0	1	Interlaced	Pipelined SD VSYNC /Field.	See Appendix 5—SD Timing.
0	0	1	x	x	Pipelined ED/HD VSYNC or field signal.	As per VSYNC or field signal timing.
1	0	1	x	All HD interlaced standards	Pipelined field signal based on AV Code F bit.	Field.
1	0	1	x	All ED/HD progressive standards	Pipelined VSYNC based on AV Code V bit.	Vertical blanking interval.
x	1	1	x	All ED/HD standards except 525p	Pipelined ED/HD VSYNC based on vertical counter.	Aligned with serration lines.
x	1	1	x	525p	Pipelined ED/HD VSYNC based on vertical counter.	Vertical blanking interval.

[1] In all ED/HD standards where there is a VSYNC output, the start of the VSYNC pulse is aligned with the falling edge of the embedded VSYNC in the output video.

LOW POWER MODE

Subaddress 0x0D, Bits[2:0]

For power sensitive applications, the ADV7342/ADV7343 support an Analog Devices, Inc. proprietary low power mode of operation on DAC 1, DAC 2, and DAC 3. To utilize this low power mode, these DACs must be operating in full-drive mode (R_{SET} = 510 Ω, R_L = 37.5 Ω). Low power mode is not available in low drive mode (R_{SET} = 4.12 kΩ, R_L = 300 Ω). Low power mode can be independently enabled or disabled on DAC 1, DAC 2, and DAC 3 using Subaddress 0x0D, Bits[2:0]. Low power mode is disabled by default on each DAC.

In low power mode, DAC current consumption is content dependent. On a typical video stream, it can be reduced by as much as 40%. For applications requiring the highest possible video performance, low power mode should be disabled.

CABLE DETECTION

Subaddress 0x10

The ADV7342/ADV7343 include an Analog Devices, Inc. proprietary cable detection feature.

The cable detection feature is available on DAC 1 and DAC 2, while operating in full-drive mode (R_{SET1} = 510 Ω, R_{L1} = 37.5 Ω, assuming a connected cable). The feature is not available in low drive mode (R_{SET} = 4.12 kΩ, R_L = 300 Ω). For a DAC to be monitored, the DAC must be powered up in Subaddress 0x00.

The cable detection feature can be used with all SD, ED, and HD video standards. It is available for all output configurations, that is, CVBS, YC, YPrPb, and RGB output configurations.

For CVBS/YC output configurations, both DAC 1 and DAC 2 are monitored, that is, the CVBS and YC luma outputs are monitored. For YPrPb and RGB output configurations, only DAC 1 is monitored, that is, the luma or green output is monitored.

Once per frame, the ADV7342/ADV7343 monitor DAC 1 and/or DAC 2, updating Subaddress 0x10, Bit 0 and Bit 1, respectively. If a cable is detected on one of the DACs, the relevant bit is set to 0. If not, the bit is set to 1.

DAC AUTO POWER-DOWN

Subaddress 0x10, Bit 4

For power sensitive applications, a DAC auto power-down feature can be enabled using Subaddress 0x10, Bit 4. This feature is only available when the cable detection feature is enabled.

With this feature enabled, the cable detection circuitry monitors DAC 1 and/or DAC 2 once per frame. If they are unconnected, some or all of the DACs automatically power down. Which DAC or DACs are powered down depends on the selected output configuration.

For CVBS/YC output configurations, if DAC 1 is unconnected, only DAC 1 powers down. If DAC 2 is unconnected, DAC 2 and DAC 3 power down.

For YPrPb and RGB output configurations, if DAC 1 is unconnected, all three DACs power down. DAC 2 is not monitored for YPrPb and RGB output configurations.

Once per frame, DAC 1 and/or DAC 2 are monitored. If a cable is detected, the appropriate DAC or DACs remain powered up for the duration of the frame. If no cable is detected, the appropriate DAC or DACs power down until the next frame, when the process is repeated.

PIXEL AND CONTROL PORT READBACK

Subaddress 0x12 to Subaddress 0x14, Subaddress 0x16

The ADV7342/ADV7343 support the readback of most digital inputs via the I²C/SPI MPU port. This feature is useful for board level connectivity testing with upstream devices.

The pixel port (S[7:0], Y[7:0], and C[7:0]), the control port ($\overline{S\_HSYNC}$, $\overline{S\_VSYNC}$, $\overline{P\_HSYNC}$, $\overline{P\_VSYNC}$ and $\overline{P\_BLANK}$), and the SFL/MISO pin are available for readback via the MPU port. The readback registers are located at Subaddress 0x12 to Subaddress 0x14 and Subaddress 0x16.

When using this feature, a clock signal should be applied to the CLKIN_A pin to register the levels applied to the input pins.

RESET MECHANISM

Subaddress 0x17, Bit 1

The ADV7342/ADV7343 have a software reset accessible via the I²C/SPI MPU port. A software reset is activated by writing a 1 to Subaddress 0x17, Bit 1. This resets all registers to their default values. This bit is self-clearing, that is, after a 1 has been written to the bit, the bit automatically returns to 0.

When operating in SPI mode, a software reset does not cause the device to revert to I²C mode. For this to occur, the ADV7342/ADV7343 need to be powered down.

The ADV7342/ADV7343 include a power-on reset (POR) circuit to ensure correct operation after power-up.

PRINTED CIRCUIT BOARD LAYOUT AND DESIGN

DAC CONFIGURATIONS

The ADV7342/ADV7343 contain six DACs. All six DACs can be configured to operate in low drive mode. Low drive mode is defined as 4.33 mA full-scale current into a 300 Ω load, R_L.

DAC 1, DAC 2, and DAC 3 can also be configured to operate in full-drive mode. Full-drive mode is defined as 34.7 mA full-scale current into a 37.5 Ω load, R_L. Full-drive is the recommended mode of operation for DAC 1, DAC 2, and DAC 3.

The ADV7342/ADV7343 contain two R_{SET} pins. A resistor connected between the R_{SET1} pin and AGND is used to control the full-scale output current and, therefore, the DAC output voltage levels of DAC 1, DAC 2, and DAC 3. For low drive operation, R_{SET1} must have a value of 4.12 kΩ, and R_L must have a value of 300 Ω. For full-drive operation, R_{SET1} must have a value of 510 Ω, and R_L must have a value of 37.5 Ω.

A resistor connected between the R_{SET2} pin and AGND is used to control the full-scale output current and, therefore, the DAC output voltage levels of DAC 4, DAC 5, and DAC 6. R_{SET2} must have a value of 4.12 kΩ, and R_L must have a value of 300 Ω (that is, low drive operation only).

The resistors connected to the R_{SET1} and R_{SET2} pins should have a 1% tolerance.

The ADV7342/ADV7343 contain two compensation pins, COMP1 and COMP2. A 2.2 nF compensation capacitor should be connected from each of these pins to V_{AA}.

VOLTAGE REFERENCE

The ADV7342/ADV7343 contain an on-chip voltage reference that can be used as a board-level voltage reference via the V_{REF} pin. Alternatively, the ADV7342/ADV7343 can be used with an external voltage reference by connecting the reference source to the V_{REF} pin. For optimal performance, an external voltage reference such as the AD1580 should be used with the ADV7342/ADV7343. If an external voltage reference is not used, a 0.1 µF capacitor should be connected from the V_{REF} pin to V_{AA}.

VIDEO OUTPUT BUFFER AND OPTIONAL OUTPUT FILTER

An output buffer is necessary on any DAC that operates in low drive mode (R_{SET} = 4.12 kΩ, R_L = 300 Ω). Analog Devices, Inc. produces a range of op amps suitable for this application, for example, the AD8061. For more information about line driver buffering circuits, see the relevant op amp data sheet.

An optional reconstruction (anti-imaging) low-pass filter (LPF) may be required on the ADV7342/ADV7343 DAC outputs if the ADV7342/ADV7343 are connected to a device that requires this filtering.

The filter specifications vary with the application. The use of 16× (SD), 8× (ED), or 4× (HD) oversampling can remove the requirement for a reconstruction filter altogether.

For applications requiring an output buffer and reconstruction filter, the ADA4430-1, ADA4411-3, and ADA4410-6 integrated video filter buffers should be considered.

Table 53. ADV7342/ADV7343 Output Rates

Input Mode (0x01, Bits[6:4])	PLL Control (0x00, Bit 1)	Output Rate (MHz)	
SD Only	Off	27	(2x)
	On	216	(16x)
ED Only	Off	27	(1x)
	On	216	(8x)
HD Only	Off	74.25	(1x)
	On	297	(4x)

Table 54. Output Filter Requirements

Application	Oversampling	Cutoff Frequency (MHz)	Attenuation –50 dB @ (MHz)
SD	2×	>6.5	20.5
SD	16×	>6.5	209.5
ED	1×	>12.5	14.5
ED	8×	>12.5	203.5
HD	1×	>30	44.25
HD	4×	>30	267

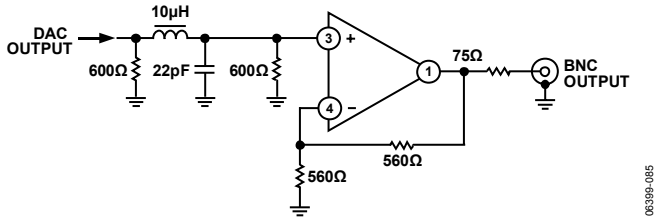


Figure 84. Example of Output Filter for SD, 16× Oversampling

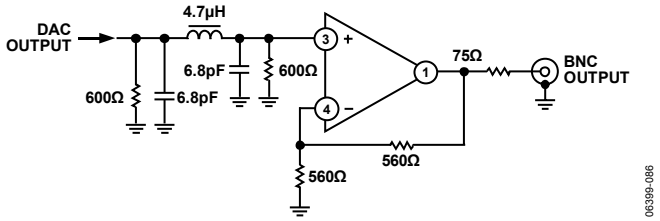


Figure 85. Example of Output Filter for ED, 8× Oversampling

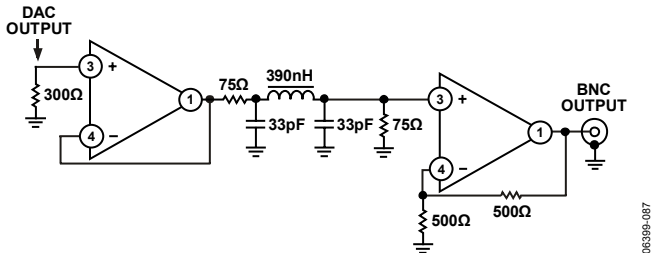


Figure 86. Example of Output Filter for HD, 4× Oversampling

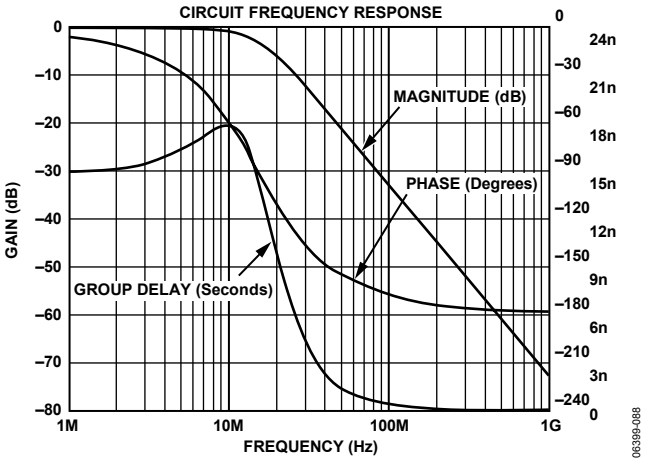


Figure 87. Output Filter Plot for SD, 16× Oversampling

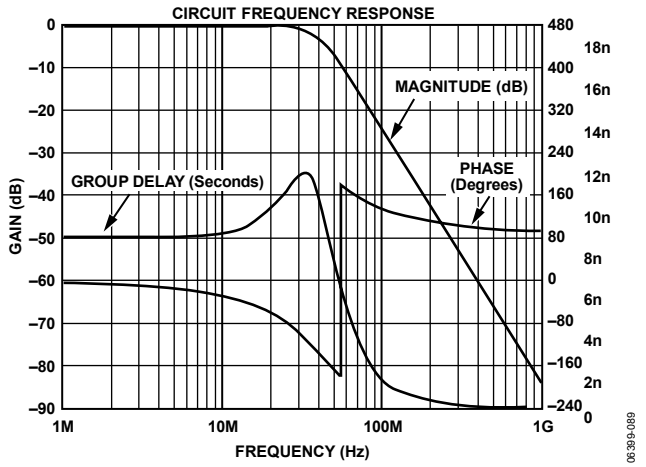


Figure 88. Output Filter Plot for ED, 8× Oversampling

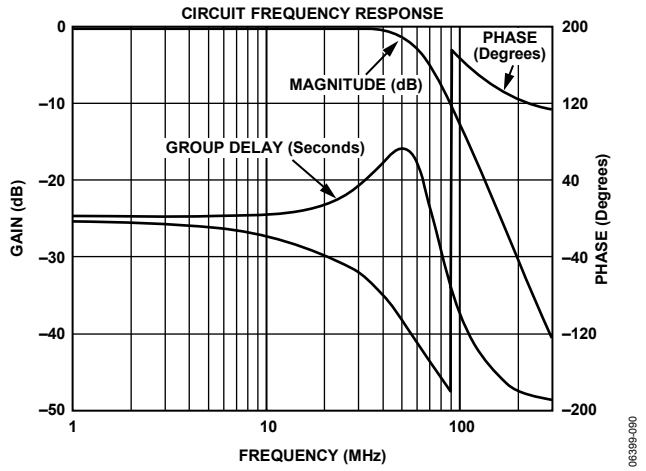


Figure 89. Output Filter Plot for HD, 4× Oversampling

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADV7342/ADV7343 are highly integrated circuits containing both precision analog and high speed digital circuitry. They have been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system-level design so that optimal performance is achieved.

The layout should be optimized for lowest noise on the ADV7342/ADV7343 power and ground planes by shielding the digital inputs and providing good power supply decoupling.

It is recommended to use a 4-layer printed circuit board with ground and power planes separating the signal trace layer and the solder side layer.

Component Placement

Component placement should be carefully considered to separate noisy circuits, such as clock signals and high speed digital circuitry from analog circuitry.

The external loop filter components and components connected to the COMP, V_{REF}, and R_{SET} pins should be placed as close as possible to and on the same side of the PCB as the ADV7342/ADV7343. Adding vias to the PCB to get the components closer to the ADV7342/ADV7343 are not recommended.

It is recommended that the ADV7342/ADV7343 be placed as close as possible to the output connector, with the DAC output traces as short as possible.

The termination resistors on the DAC output traces should be placed as close as possible to and on the same side of the PCB as the ADV7342/ADV7343. The termination resistors should overlay the PCB ground plane.

External filter and buffer components connected to the DAC outputs should be placed as close as possible to the ADV7342/ADV7343 to minimize the possibility of noise pickup from neighboring circuitry, and to minimize the effect of trace capacitance on output bandwidth. This is particularly important when operating in low drive mode (R_{SET} = 4.12 kΩ, R_L = 300 Ω).

Power Supplies

It is recommended that a separate regulated supply be provided for each power domain (V_{AA}, V_{DD}, V_{DD_IO}, and PV_{DD}). For optimal performance, linear regulators rather than switch mode regulators should be used. If switch mode regulators must be used, care must be taken with regard to the quality of the output voltage in terms of ripple and noise. This is particularly true for the V_{AA} and PV_{DD} power domains. Each power supply should be individually connected to the system power supply at a single point through a suitable filtering device, such as a ferrite bead.

Power Supply Decoupling

It is recommended that each power supply pin be decoupled with 10 nF and 0.1 µF ceramic capacitors. The V_{AA}, PV_{DD}, V_{DD_IO}, and both V_{DD} pins should be individually decoupled to ground. The decoupling capacitors should be placed as close as possible to the ADV7342/ADV7343 with the capacitor leads kept as short as possible to minimize lead inductance.

A 1 µF tantalum capacitor is recommended across the V_{AA} supply in addition to the 10 nF and 0.1 µF ceramic capacitors.

Power Supply Sequencing

The ADV7342/ADV7343 are robust to all power supply sequencing combinations. Any particular sequence can be used.

Digital Signal Interconnect

The digital signal traces should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal traces should not overlay the V_{AA} or PV_{DD} power planes.

Due to the high clock rates used, avoid long clock traces to the ADV7342/ADV7343 to minimize noise pickup.

Any pull-up termination resistors for the digital inputs should be connected to the V_{DD} power supply.

Any unused digital inputs should be tied to ground.

Analog Signal Interconnect

DAC output traces should be treated as transmission lines with appropriate measures taken to ensure optimal performance (for example, impedance matched traces). The DAC output traces should be kept as short as possible. The termination resistors on the DAC output traces should be placed as close as possible to and on the same side of the PCB as the ADV7342/ADV7343.

To avoid crosstalk between the DAC outputs, it is recommended that as much space as possible be left between the traces connected to the DAC output pins. Adding ground traces between the DAC output traces is also recommended.

TYPICAL APPLICATION CIRCUIT

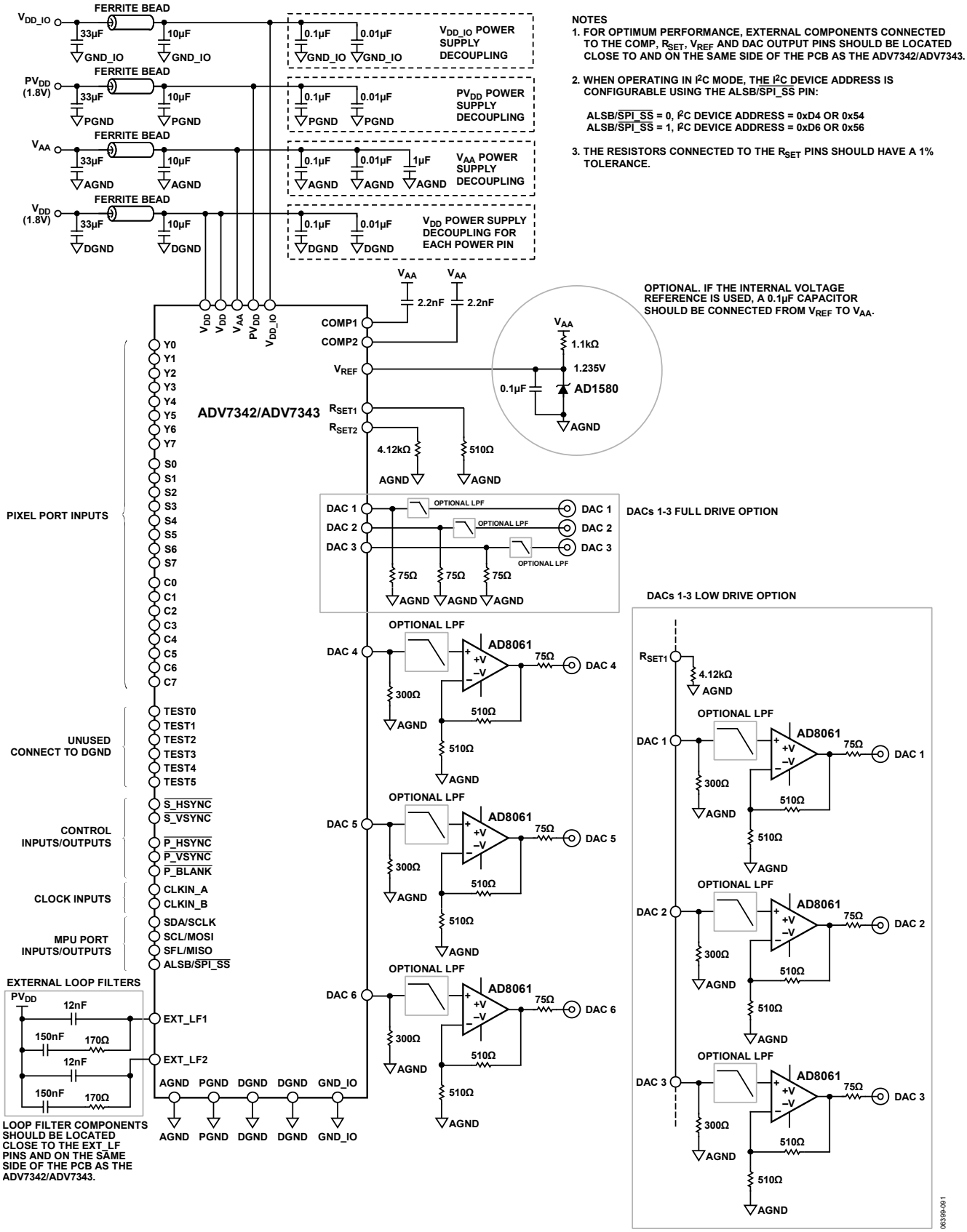


Figure 90. ADV7342/ADV7343 Typical Application Circuit

APPENDIX 1—COPY GENERATION MANAGEMENT SYSTEM

SD CGMS

Subaddress 0x99 to Subaddress 0x9B

The ADV7342/ADV7343 support copy generation management system (CGMS) conforming to the EIAJ CPR-1204 and ARIB TR-B15 standards. CGMS data is transmitted on Line 20 of the odd fields and Line 283 of even fields. Subaddress 0x99, Bits[6:5] control whether CGMS data is output on odd or even fields or both.

SD CGMS data can only be transmitted when the ADV7342/ADV7343 are configured in NTSC mode. The CGMS data is 20 bits long. The CGMS data is preceded by a reference pulse of the same amplitude and duration as a CGMS bit (see Figure 91).

ED CGMS

Subaddress 0x41 to Subaddress 0x43
Subaddress 0x5E to Subaddress 0x6E

525p

The ADV7342/ADV7343 support copy generation management system (CGMS) in 525p mode in accordance with EIAJ CPR-1204-1.

When ED CGMS is enabled (Subaddress 0x32, Bit 6 = 1), 525p CGMS data is inserted on Line 41. The 525p CGMS data registers are at Subaddress 0x41, Subaddress 0x42, and Subaddress 0x43.

The ADV7342/ADV7343 also support CGMS Type B packets in 525p mode in accordance with CEA-805-A.

When ED CGMS Type B is enabled (Subaddress 0x5E, Bit 0 = 1), 525p CGMS Type B data is inserted on Line 40. The 525p CGMS Type B data registers are at Subaddress 0x5E to Subaddress 0x6E.

625p

The ADV7342/ADV7343 support copy generation management system (CGMS) in 625p mode in accordance with IEC62375 (2004).

When ED CGMS is enabled (Subaddress 0x32, Bit 6 = 1), 625p CGMS data is inserted on Line 43. The 625p CGMS data registers are at Subaddress 0x42 and Subaddress 0x43.

HD CGMS

Subaddress 0x41 to Subaddress 0x43
Subaddress 0x5E to Subaddress 0x6E

The ADV7342/ADV7343 support copy generation management system (CGMS) in HD mode (720p and 1080i) in accordance with EIAJ CPR-1204-2.

When HD CGMS is enabled (Subaddress 0x32, Bit 6 = 1), 720p CGMS data is applied to Line 24 of the luminance vertical blanking interval.

When HD CGMS is enabled (Subaddress 0x32, Bit 6 = 1), 1080i CGMS data is applied to Line 19 and Line 582 of the luminance vertical blanking interval.

The HD CGMS data registers are at Subaddress 0x41, Subaddress 0x42, and Subaddress 0x43.

The ADV7342/ADV7343 also support CGMS Type B packets in HD mode (720p and 1080i) in accordance with CEA-805-A.

When HD CGMS Type B is enabled (Subaddress 0x5E, Bit 0 = 1), 720p CGMS data is applied to Line 23 of the luminance vertical blanking interval.

When HD CGMS Type B is enabled (Subaddress 0x5E, Bit 0 = 1), 1080i CGMS data is applied to Line 18 and Line 581 of the luminance vertical blanking interval.

The HD CGMS Type B data registers are at Subaddress 0x5E to Subaddress 0x6E.

CGMS CRC FUNCTIONALITY

If SD CGMS CRC (Subaddress 0x99, Bit 4) or ED/HD CGMS CRC (Subaddress 0x32, Bit 7) is enabled, the upper six CGMS data bits, C19 to C14, which comprise the 6-bit CRC check sequence, are automatically calculated on the ADV7342/ADV7343. This calculation is based on the lower 14 bits (C13 to C0) of the data in the CGMS data registers and the result is output with the remaining 14 bits to form the complete 20 bits of the CGMS data. The calculation of the CRC sequence is based on the polynomial $x^6 + x + 1$ with a preset value of 111111.

If SD CGMS CRC or ED/HD CGMS CRC are disabled, all 20 bits (C19 to C0) are output directly from the CGMS registers (CRC must be calculated by the user manually).

If ED/HD CGMS Type B CRC (Subaddress 0x5E, Bit 1) is enabled, the upper six CGMS Type B data bits (P122 to P127) that comprise the 6-bit CRC check sequence are automatically calculated on the ADV7342/ADV7343. This calculation is based on the lower 128 bits (H0 to H5 and P0 to P121) of the data in the CGMS Type B data registers. The result is output with the remaining 128 bits to form the complete 134 bits of the CGMS Type B data. The calculation of the CRC sequence is based on the polynomial $x^6 + x + 1$ with a preset value of 111111.

If ED/HD CGMS Type B CRC is disabled, all 134 bits (H0 to H5 and P0 to P127) are output directly from the CGMS Type B registers (CRC must be calculated by the user manually).

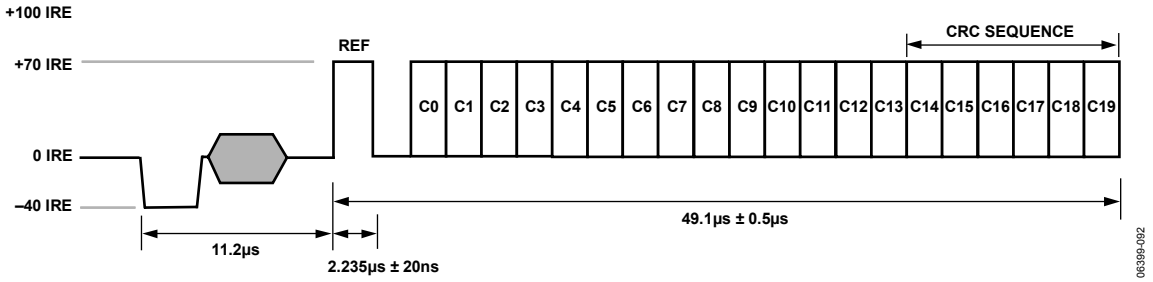


Figure 91. Standard Definition CGMS Waveform

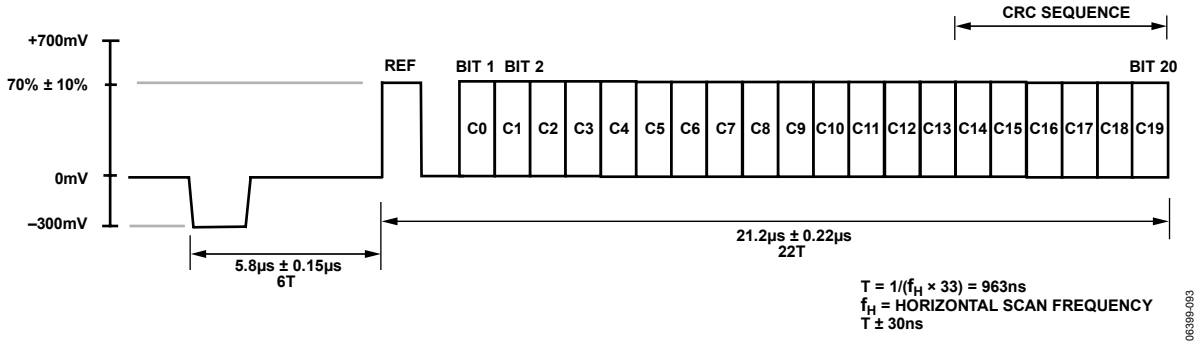


Figure 92. Enhanced Definition (525p) CGMS Waveform

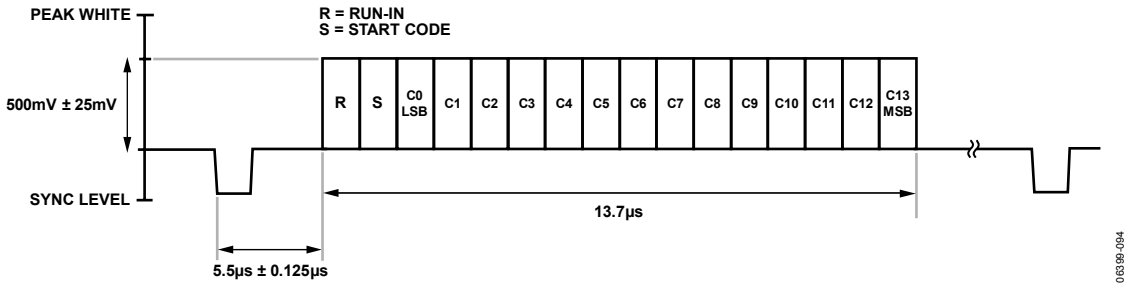


Figure 93. Enhanced Definition (625p) CGMS Waveform

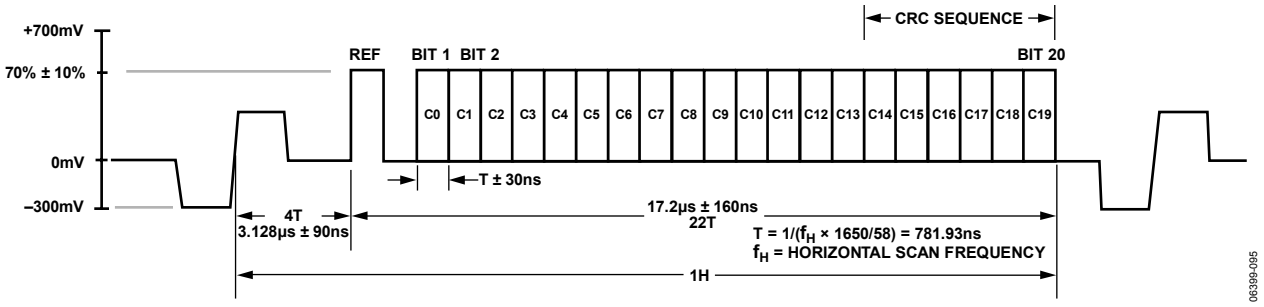


Figure 94. High Definition (720p) CGMS Waveform

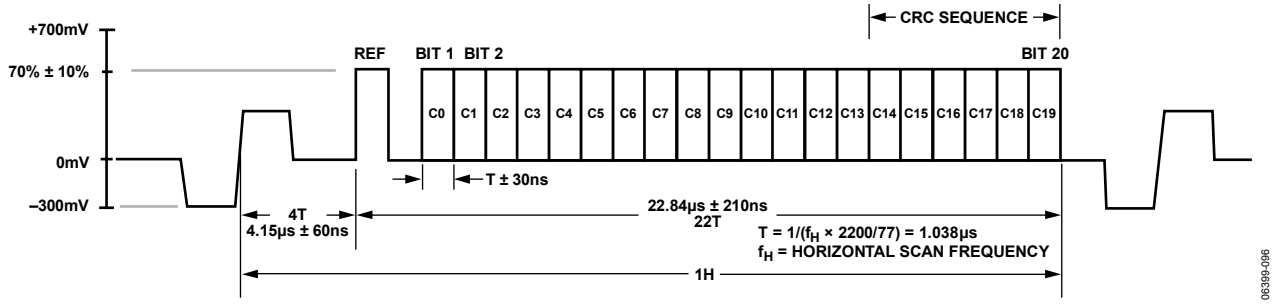
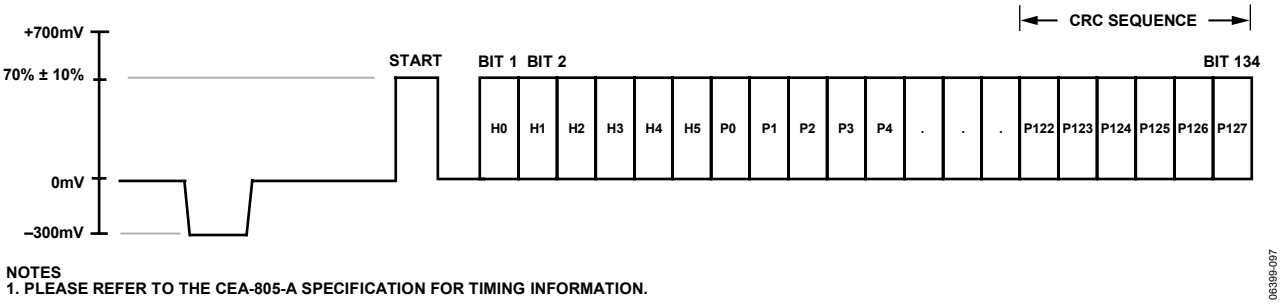
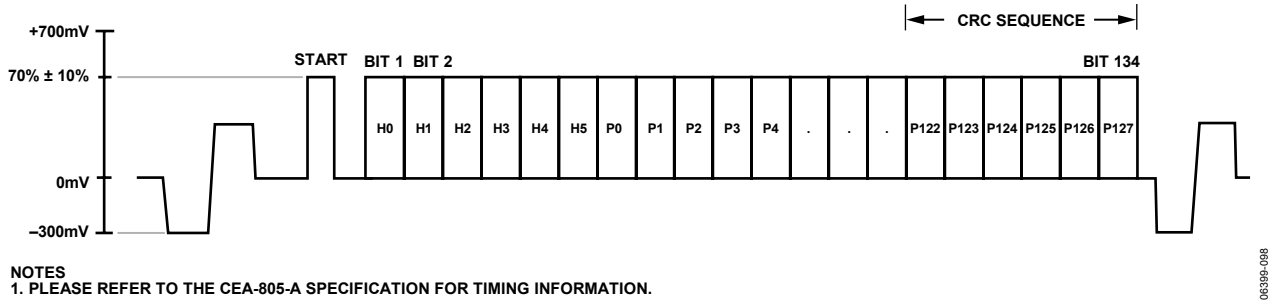


Figure 95. High Definition (1080i) CGMS Waveform



NOTES
1. PLEASE REFER TO THE CEA-805-A SPECIFICATION FOR TIMING INFORMATION.

Figure 96. Enhanced Definition (525p) CGMS Type B Waveform



NOTES
1. PLEASE REFER TO THE CEA-805-A SPECIFICATION FOR TIMING INFORMATION.

Figure 97. High Definition (720p and 1080i) CGMS Type B Waveform

APPENDIX 2—SD WIDE SCREEN SIGNALING

Subaddress 0x99, Subaddress 0x9A, Subaddress 0x9B

The ADV7342/ADV7343 support wide screen signaling (WSS) conforming to the ETSI 300 294 standard. WSS data is transmitted on Line 23. WSS data can be transmitted only when the device is configured in PAL mode. The WSS data is 14 bits long. The function of each of these bits is shown in Table 55. The WSS data is preceded by a run-in sequence and a start code (see Figure 98). The latter portion of Line 23 (after 42.5 µs from the falling edge of $\overline{\text{HSYNC}}$) is available for the insertion of video. WSS data transmission on Line 23 can be enabled using Subaddress 0x99, Bit 7. It is possible to blank the WSS portion of Line 23 with Subaddress 0xA1, Bit 7.

Table 55. Function of WSS

	Bit Number														
Bit Description	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Setting**
Aspect Ratio, Format, Position											1	0	0	0	4:3, full format, N/A
											0	0	0	1	14:9, letterbox, center
											0	0	1	0	14:9, letterbox, top
											1	0	1	1	16:9, letterbox, center
											0	1	0	0	16:9, letterbox, top
											1	1	0	1	>16:9, letterbox, center
											1	1	1	0	14:9, full format, center
											0	1	1	1	16:0, N/A, N/A
Mode										0					Camera mode
										1					Film mode
Color Encoding									0						Normal PAL
									1						Motion Adaptive ColorPlus
Helper Signals								0							Not present
								1							Present
Reserved							0								
Teletext Subtitles						0									No
						1									Yes
Open Subtitles				0	0										No
				0	1										Subtitles in active image area
				1	0										Subtitles out of active image area
				1	1										Reserved
Surround Sound			0												No
			1												Yes
Copyright		0													No copyright asserted or unknown
		1													Copyright asserted
Copy Protection	0														Copying not restricted
	1														Copying restricted

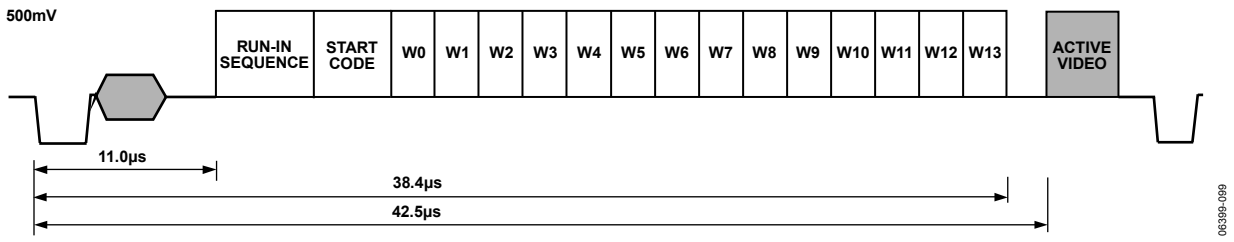


Figure 98. WSS Waveform Diagram

APPENDIX 3—SD CLOSED CAPTIONING

Subaddress 0x91 to Subaddress 0x94

The ADV7342/ADV7343 support closed captioning conforming to the standard television synchronizing waveform for color transmission. Closed captioning is transmitted during the blanked active line time of Line 21 of the odd fields and Line 284 of the even fields.

Closed captioning consists of a 7-cycle sinusoidal burst that is frequency- and phase-locked to the caption data. After the clock run-in signal, the blanking level is held for two data bits and is followed by the Logic 1 start bit. Sixteen bits of data follow the start bit. These consist of two 8-bit bytes, seven data bits, and one odd parity bit. The data for these bytes is stored in the SD closed captioning registers (Subaddress 0x93 to Subaddress 0x94).

The ADV7342/ADV7343 also support the extended closed captioning operation, which is active during even fields and encoded on Scan Line 284. The data for this operation is stored in the SD closed captioning registers (Subaddress 0x91 to Subaddress 0x92).

The ADV7342/ADV7343 automatically generate all clock run-in signals and timing that support closed captioning on Line 21 and Line 284. All pixels inputs are ignored on Line 21 and Line 284 if closed captioning is enabled.

The FCC Code of Federal Regulations (CFR) 47 Section 15.119 and EIA608 describe the closed captioning information for Line 21 and Line 284.

The ADV7342/ADV7343 use a single buffering method. This means that the closed captioning buffer is only 1-byte deep. Therefore, there is no frame delay in outputting the closed captioning data, unlike other 2-byte deep buffering systems. The data must be loaded one line before it is output on Line 21 and Line 284. A typical implementation of this method is to use $\overline{\text{VSYNC}}$ to interrupt a microprocessor, which in turn loads the new data (2 bytes) in every field. If no new data is required for transmission, 0s must be inserted in both data registers; this is called nulling. It is also important to load control codes, all of which are double bytes, on Line 21. Otherwise, a TV does not recognize them. If there is a message such as "Hello World" that has an odd number of characters, it is important to add a blank character at the end to make sure that the end-of-caption, 2-byte control code lands in the same field.

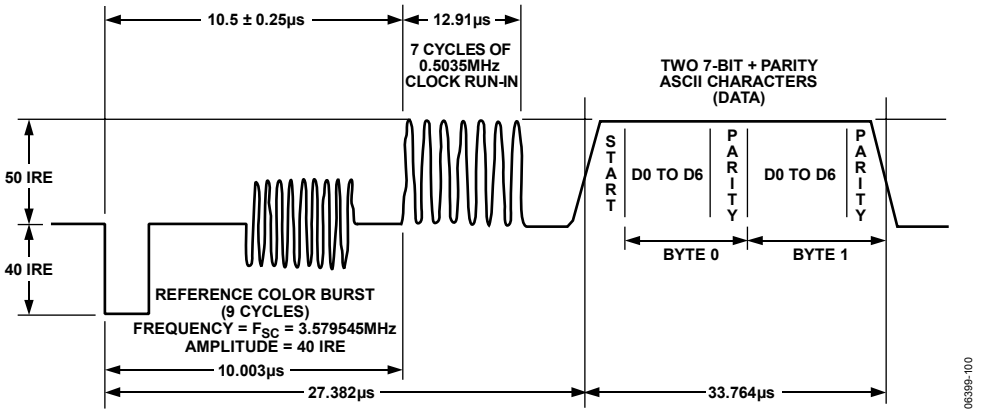


Figure 99. SD Closed Captioning Waveform, NTSC

APPENDIX 4—INTERNAL TEST PATTERN GENERATION

SD TEST PATTERNS

The ADV7342/ADV7343 are able to generate SD color bar and black bar test patterns.

The register settings in Table 56 are used to generate an SD NTSC 75% color bar test pattern. CVBS output is available on DAC 4, S-Video (Y/C) output is on DAC 5 and DAC 6, and YPrPb output is on DAC 1 to DAC 3. Upon power-up, the subcarrier frequency registers default to the appropriate values for NTSC. All other registers are set as normal/default.

Table 56. SD NTSC Color Bar Test Pattern Register Writes

Subaddress	Setting
0x00	0xFC
0x82	0xC9
0x84	0x40

To generate an SD NTSC black bar test pattern, the same settings shown in Table 56 should be used with an additional write of 0x24 to Subaddress 0x02.

For PAL output of either test pattern, the same settings are used, except that Subaddress 0x80 is programmed to 0x11 and the subcarrier frequency registers are programmed as shown in Table 57.

Table 57. PAL F_{SC} Register Writes

Subaddress	Description	Setting
0x8C	$F_{SC}0$	0xCB
0x8D	$F_{SC}1$	0x8A
0x8E	$F_{SC}2$	0x09
0x8F	$F_{SC}3$	0x2A

Note that when programming the F_{SC} registers, the user must write the values in the sequence $F_{SC}0$, $F_{SC}1$, $F_{SC}2$, $F_{SC}3$. The full F_{SC} value to be written is accepted only after the $F_{SC}3$ write is complete.

ED/HD TEST PATTERNS

The ADV7342/ADV7343 are able to generate ED/HD color bar, black bar, and hatch test patterns.

The register settings in Table 58 are used to generate an ED 525p hatch test pattern. YPrPb output is available on DAC 1 to DAC 3. All other registers are set as normal/default.

Table 58. ED 525p Hatch Test Pattern Register Writes

Subaddress	Setting
0x00	0x1C
0x01	0x10
0x31	0x05

To generate an ED 525p black bar test pattern, the same settings as shown in Table 58 should be used with an additional write of 0x24 to Subaddress 0x02.

To generate an ED 525p flat field test pattern, the same settings shown in Table 58 should be used, except that 0x0D should be written to Subaddress 0x31.

The Y, Cr, and Cb levels for the hatch and flat field test patterns can be controlled using Subaddress 0x36, Subaddress 0x37, and Subaddress 0x38, respectively.

For ED/HD standards other than 525p, the same settings as shown in Table 58 (and subsequent comments) are used except that Subaddress 0x30, Bits[7:3] are updated as appropriate.

APPENDIX 5—SD TIMING

Mode 0 (CCIR-656)—Slave Option (Subaddress 0x8A = X X X X X 0 0 0)

The ADV7342/ADV7343 are controlled by the SAV (start of active video) and EAV (end of active video) time codes embedded in the pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. If the S_VSYNC and S_HSYNC pins are not used, they should be tied high during this mode.

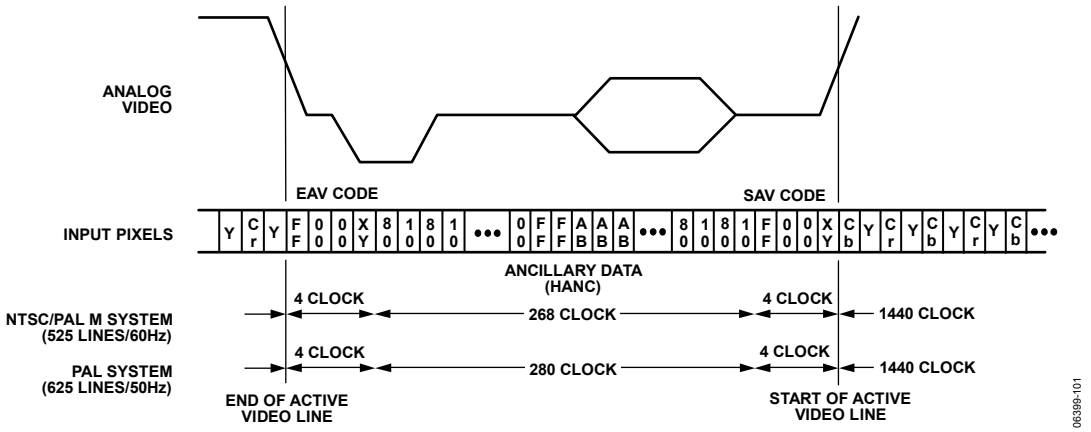


Figure 100. SD Slave Mode 0

Mode 0 (CCIR-656)—Master Option (Subaddress 0x8A = X X X X X 0 0 1)

The ADV7342/ADV7343 generate H and F signals required for the SAV and EAV time codes in the CCIR656 standard. The H bit is output on S_HSYNC and the F bit is output on S_VSYNC.

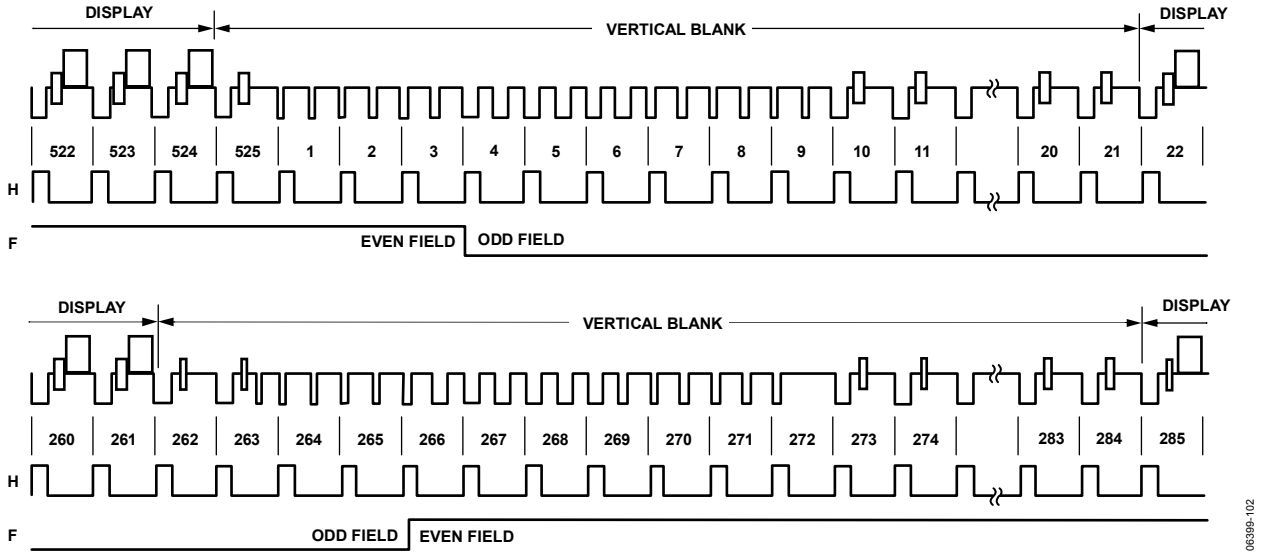


Figure 101. SD Master Mode 0, NTSC

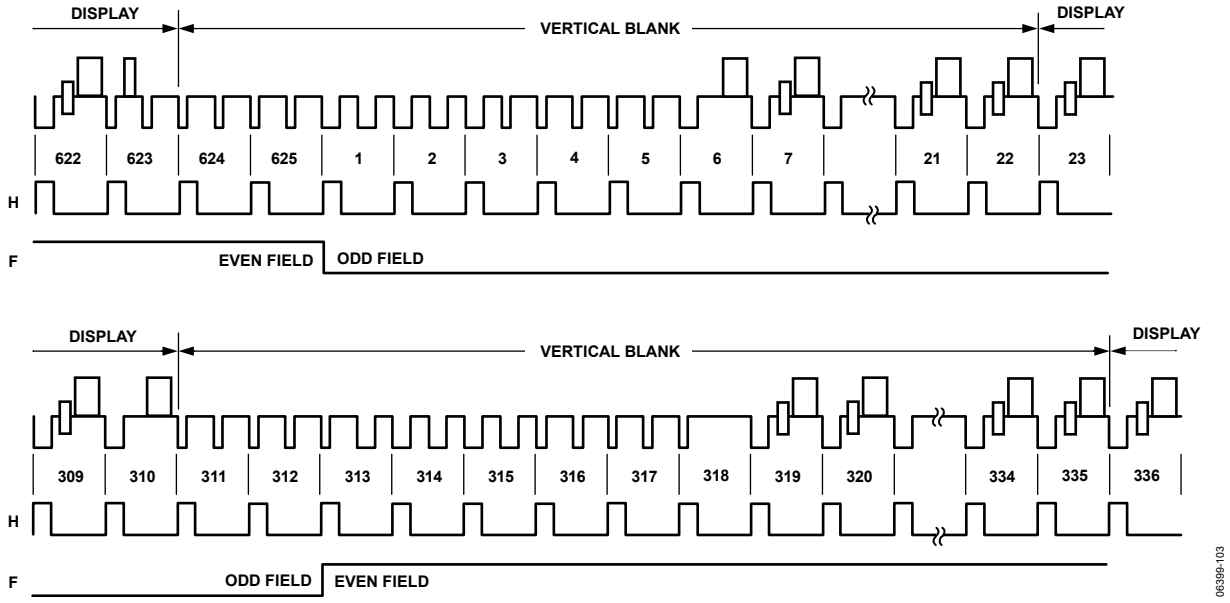


Figure 102. SD Master Mode 0, PAL

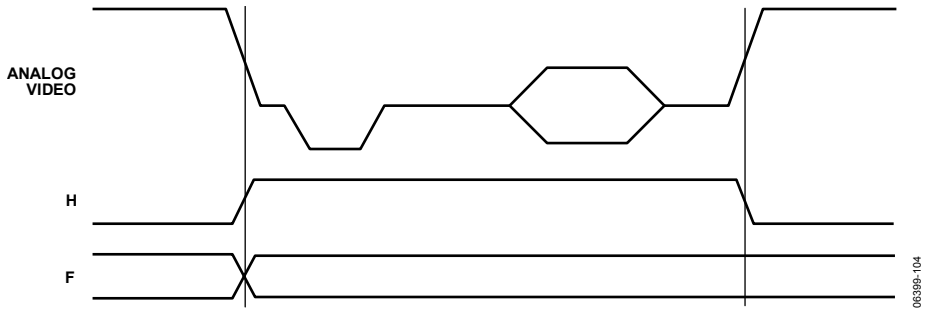


Figure 103. SD Master Mode 0, Data Transitions

Mode 1—Slave Option (Subaddress 0x8A = X X X X 0 1 0)

In this mode, the ADV7342/ADV7343 accept horizontal sync and odd/even field signals. When $\overline{\text{HSYNC}}$ is low, a transition of the field input indicates a new frame, that is, vertical retrace. The ADV7342/ADV7343 automatically blank all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$ and FIELD are input on the $\overline{\text{S\_HSYNC}}$ and $\overline{\text{S\_VSYNC}}$ pins, respectively.

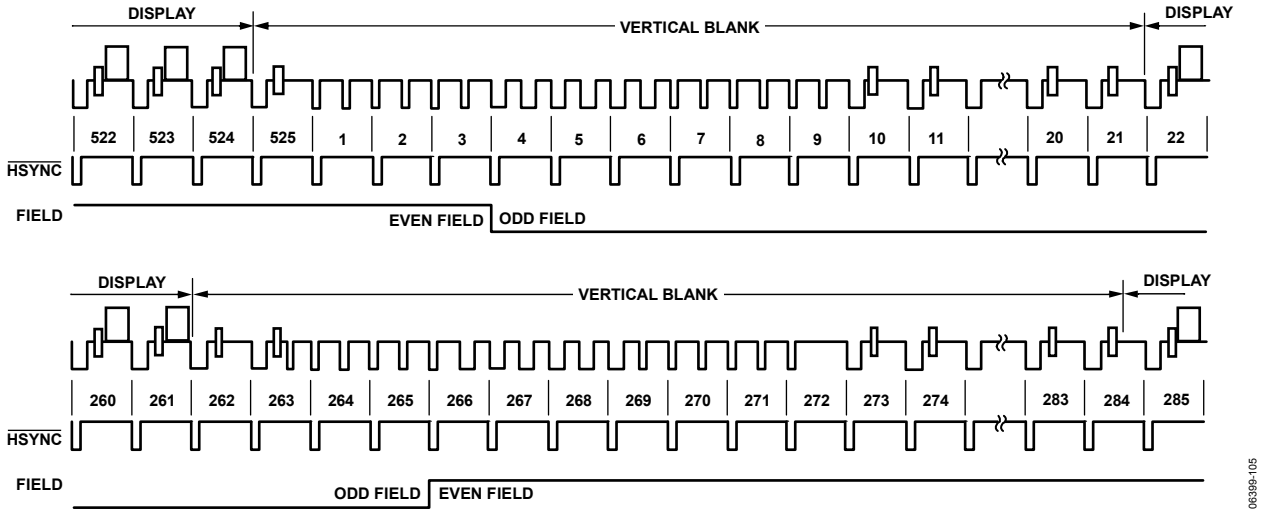


Figure 104. SD Slave Mode 1, NTSC

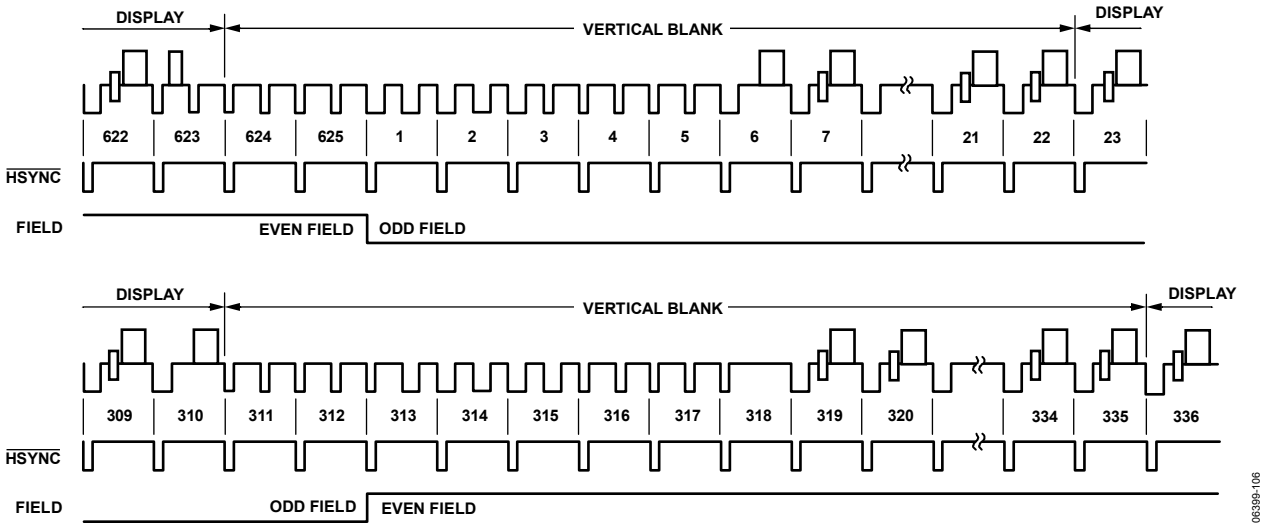


Figure 105. SD Slave Mode 1, PAL

Mode 1—Master Option (Subaddress 0x8A = X X X X X 0 1 1)

In this mode, the ADV7342/ADV7343 can generate horizontal sync and odd/even field signals. When $\overline{\text{HSYNC}}$ is low, a transition of the field input indicates a new frame, that is, vertical retrace. The ADV7342/ADV7343 automatically blank all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. $\overline{\text{HSYNC}}$ and FIELD are output on the $\overline{\text{S\_HSYNC}}$ and $\overline{\text{S\_VSYNC}}$ pins, respectively.

Figure 106. SD Timing Mode 1, Odd/Even Field Transitions (Master/Slave)

Mode 2— Slave Option (Subaddress 0x8A = X X X X X 1 0 0)

In this mode, the ADV7342/ADV7343 accept horizontal and vertical sync signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The ADV7342/ADV7343 automatically blank all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are input on the $\overline{\text{S\_HSYNC}}$ and $\overline{\text{S\_VSYNC}}$ pins, respectively.

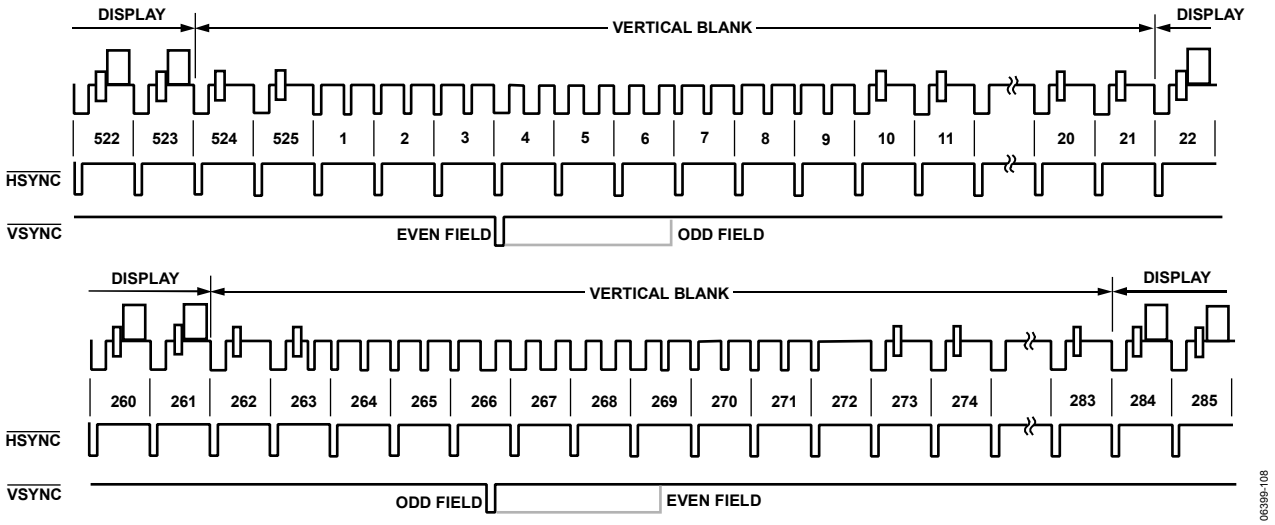


Figure 107. SD Slave Mode 2, NTSC

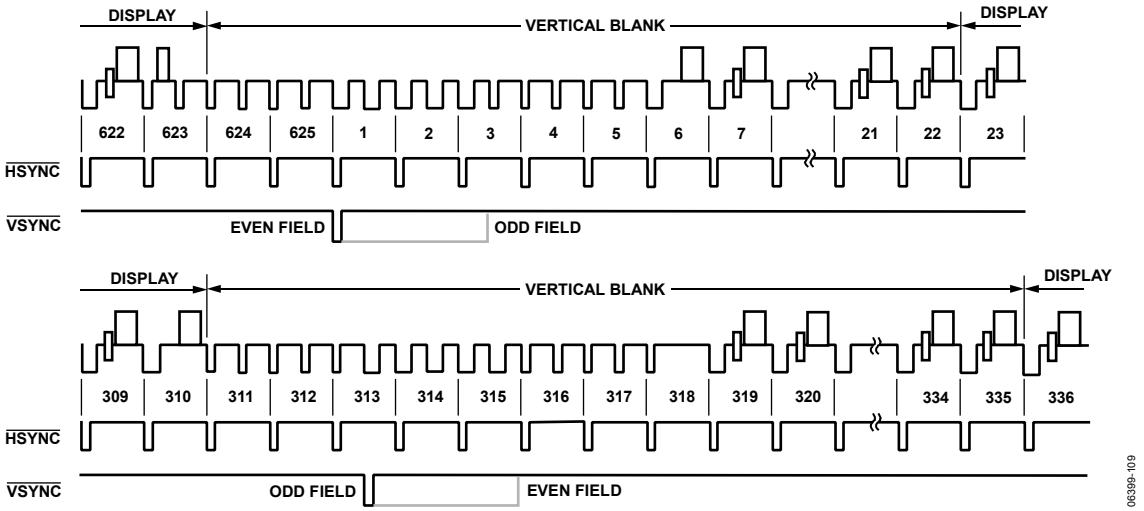


Figure 108. SD Slave Mode 2, PAL

Mode 2—Master Option (Subaddress 0x8A = X X X X X 1 0 1)

In this mode, the ADV7342/ADV7343 can generate horizontal and vertical sync signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field.

A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The ADV7342/ADV7343 automatically blank all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are output on the $\overline{\text{S\_HSYNC}}$ and $\overline{\text{S\_VSYNC}}$ pins, respectively.

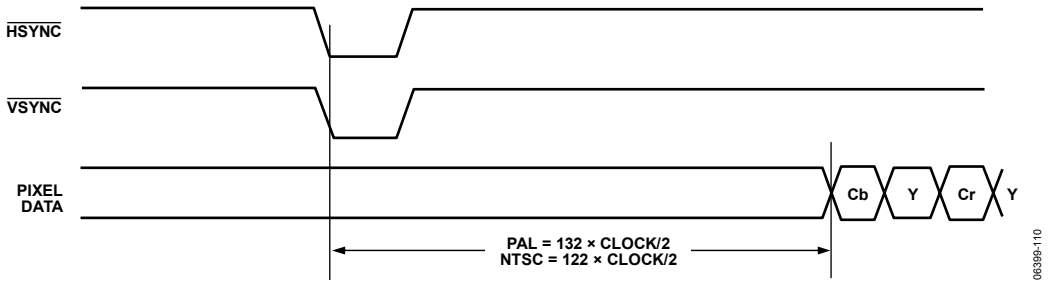


Figure 109. SD Timing Mode 2, Even-to-Odd Field Transition (Master/Slave)

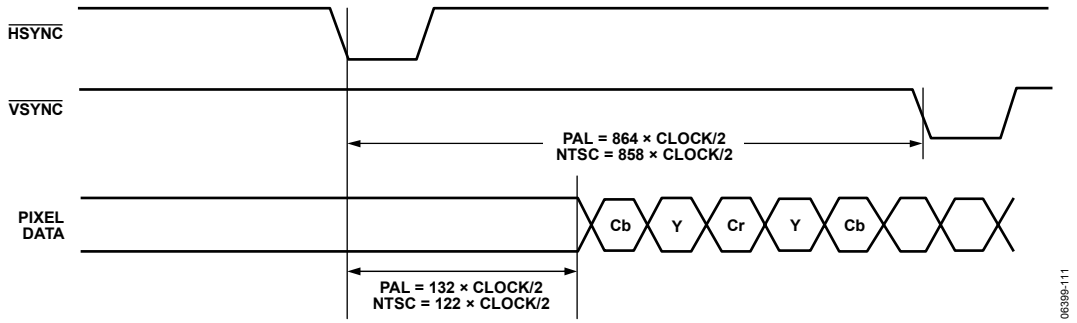


Figure 110. SD Timing Mode 2 Odd-to-Even Field Transition (Master/Slave)

Mode 3—Master/Slave Option (Subaddress 0x8A = X X X X X 1 1 0 or X X X X X 1 1 1)

In this mode, the ADV7342/ADV7343 accept or generate horizontal sync and odd/even field signals. When $\overline{\text{HSYNC}}$ is high, a transition of the field input indicates a new frame, that is, vertical retrace. The ADV7342/ADV7343 automatically blank all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are output in master mode and input in slave mode on the $\overline{\text{S\_VSYNC}}$ and $\overline{\text{S\_VSYNC}}$ pins, respectively.

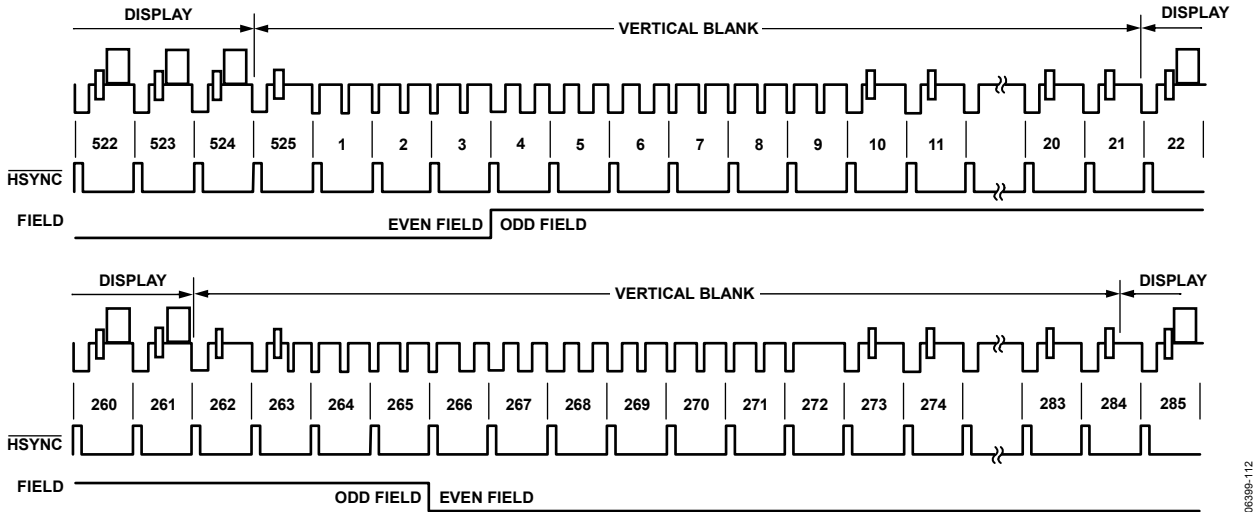


Figure 111. SD Timing Mode 3, NTSC

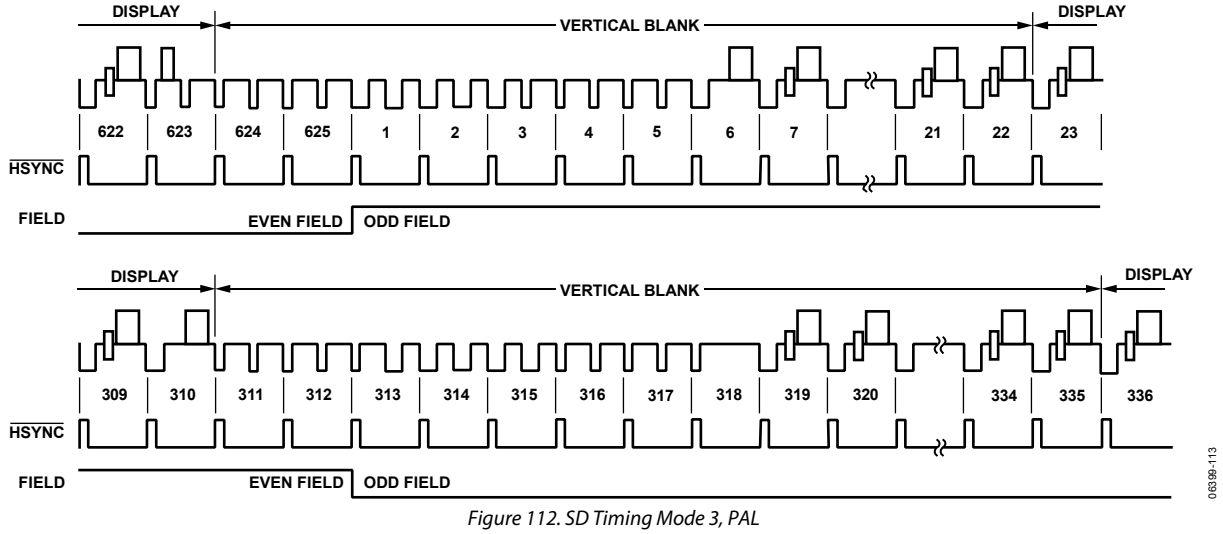


Figure 112. SD Timing Mode 3, PAL

APPENDIX 6—HD TIMING

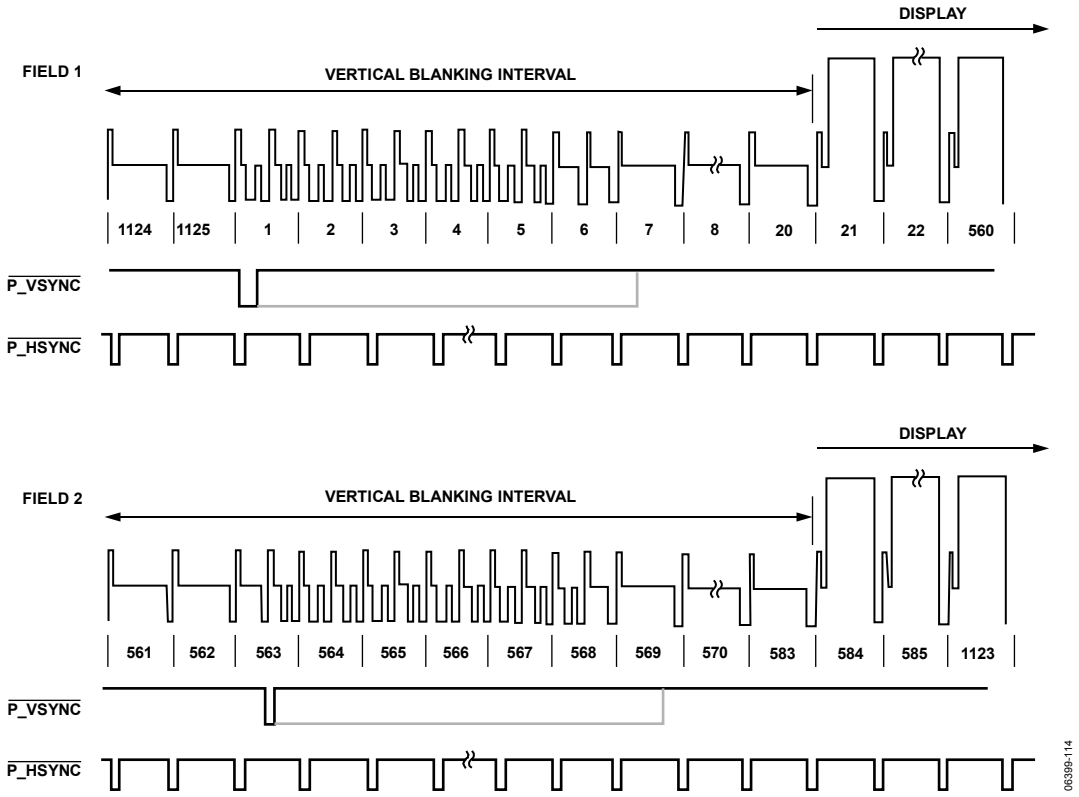


Figure 113. 1080i $\overline{HSYNC}$ and $\overline{VSYNC}$ Input Timing

APPENDIX 7—VIDEO OUTPUT LEVELS

SD YPrPb OUTPUT LEVELS—SMPTE/EBU N10

Pattern: 100% Color Bars

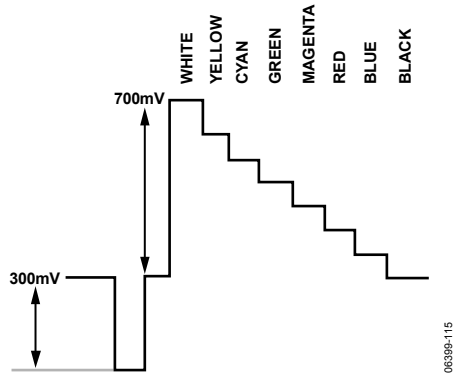


Figure 114. Y Levels—NTSC

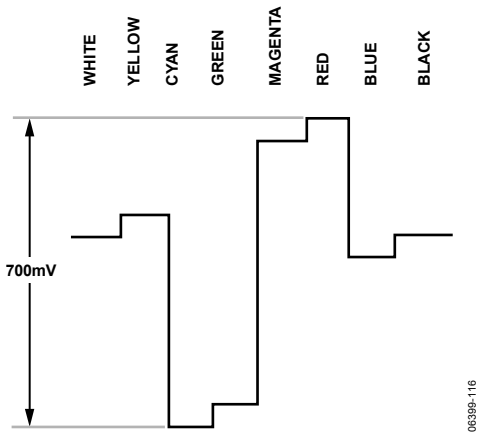


Figure 115. Pr Levels—NTSC

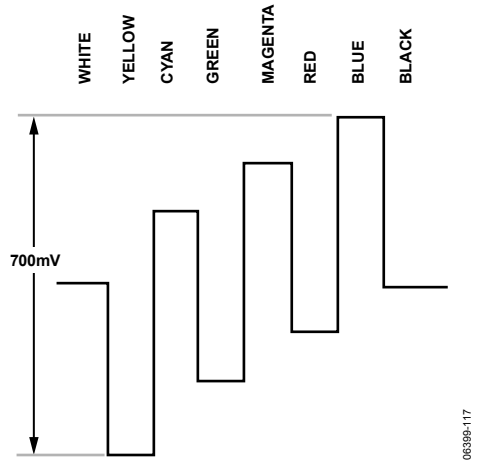


Figure 116. Pb Levels—NTSC

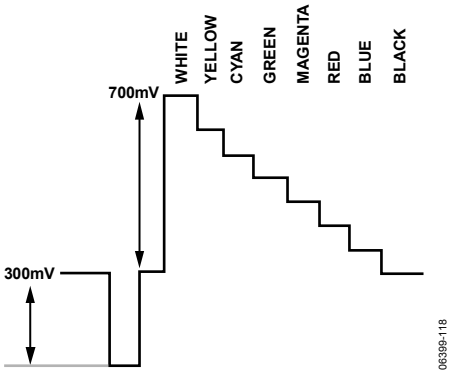


Figure 117. Y Levels—PAL

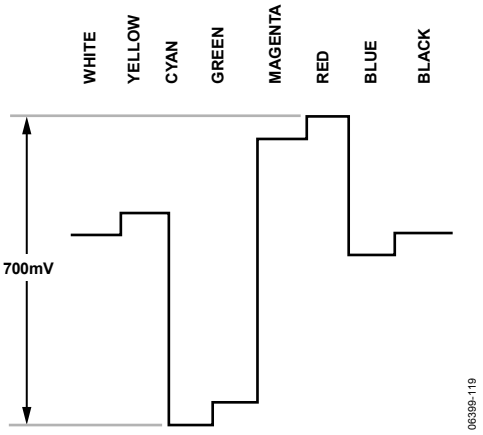


Figure 118. Pr Levels—PAL

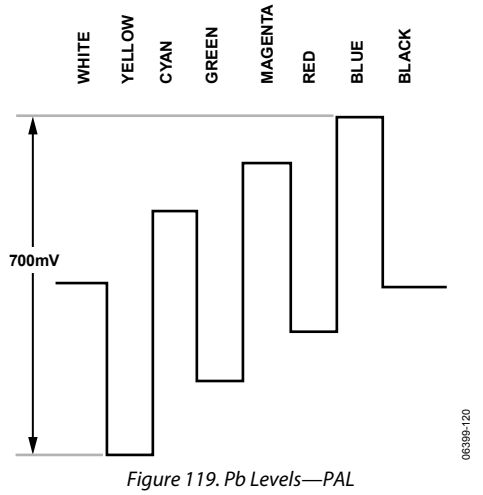


Figure 119. Pb Levels—PAL

ED/HD YPrPb OUTPUT LEVELS

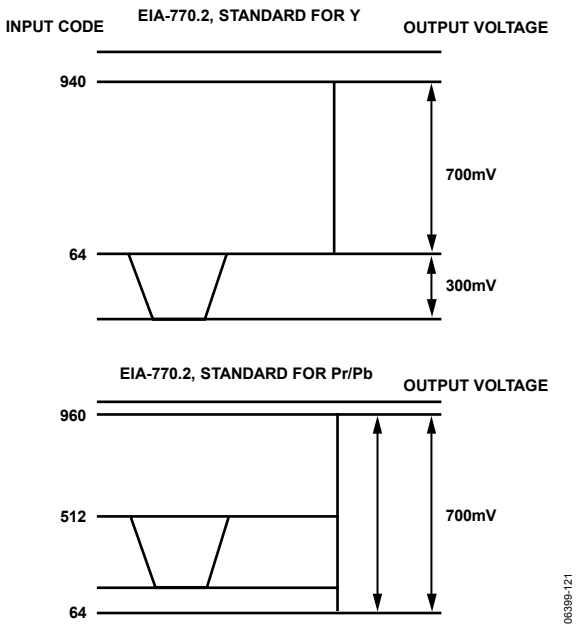


Figure 120. EIA-770.2 Standard Output Signals (525p/625p)

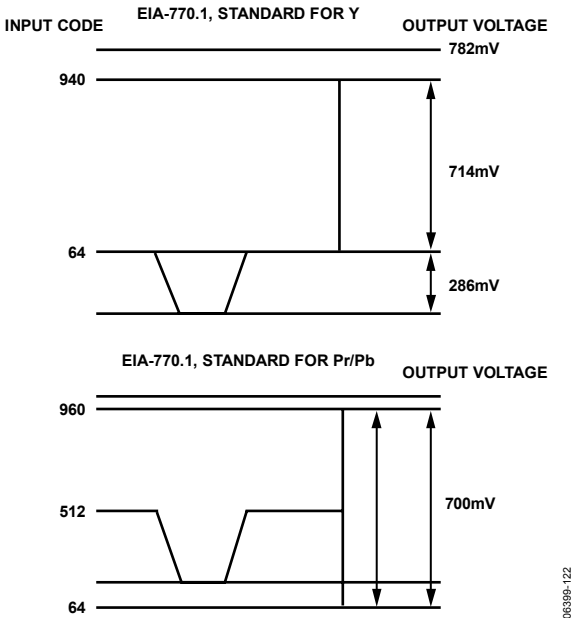


Figure 121. EIA-770.1 Standard Output Signals (525p/625p)

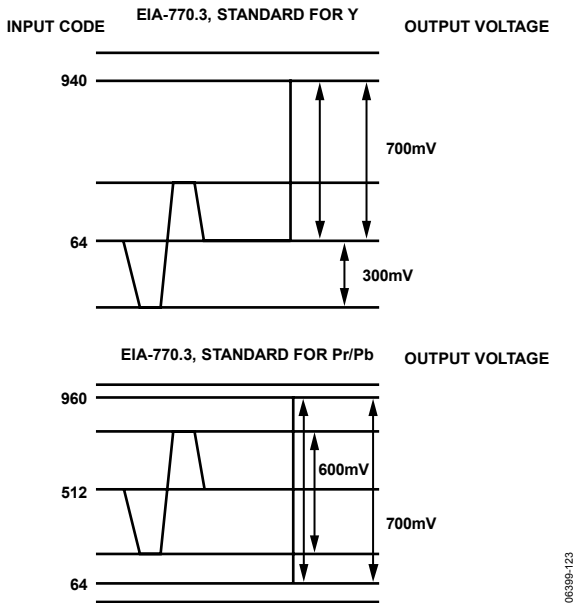


Figure 122. EIA-770.3 Standard Output Signals (1080i/720p)

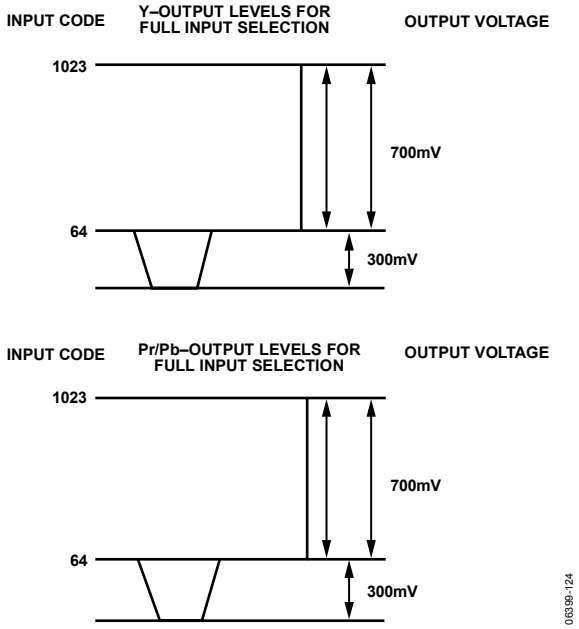


Figure 123. Output Levels for Full Input Selection

SD/ED/HD RGB OUTPUT LEVELS

Pattern: 100%/75% Color Bars

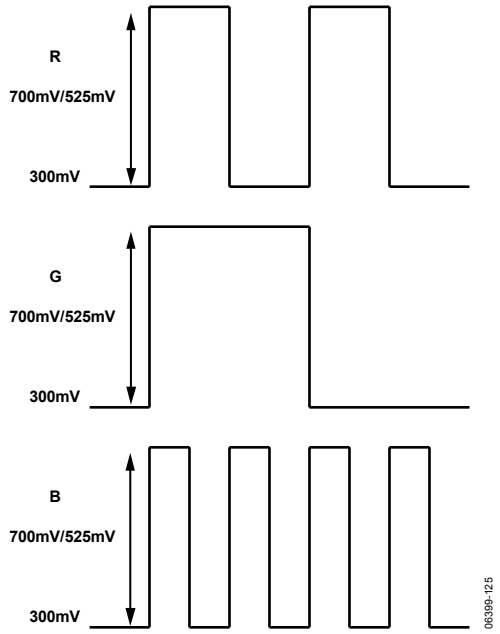


Figure 124. SD/ED RGB Output Levels—RGB Sync Disabled

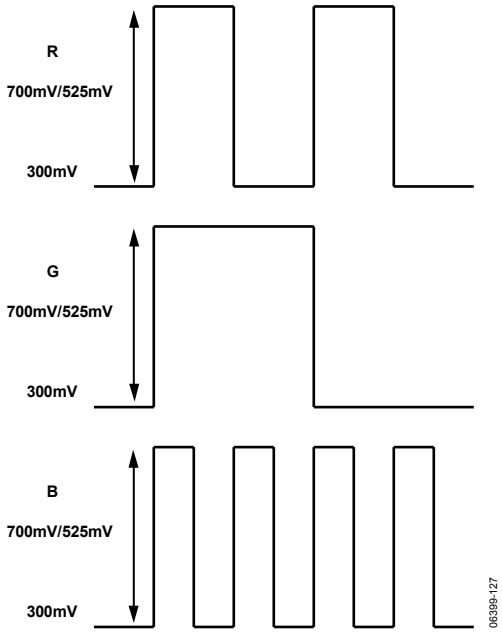


Figure 126. HD RGB Output Levels—RGB Sync Disabled

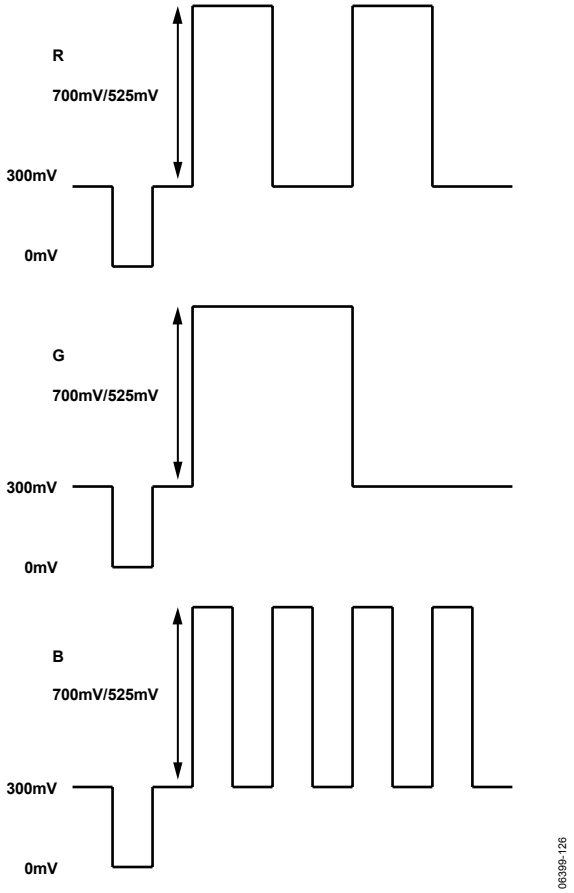


Figure 125. SD/ED RGB Output Levels—RGB Sync Enabled

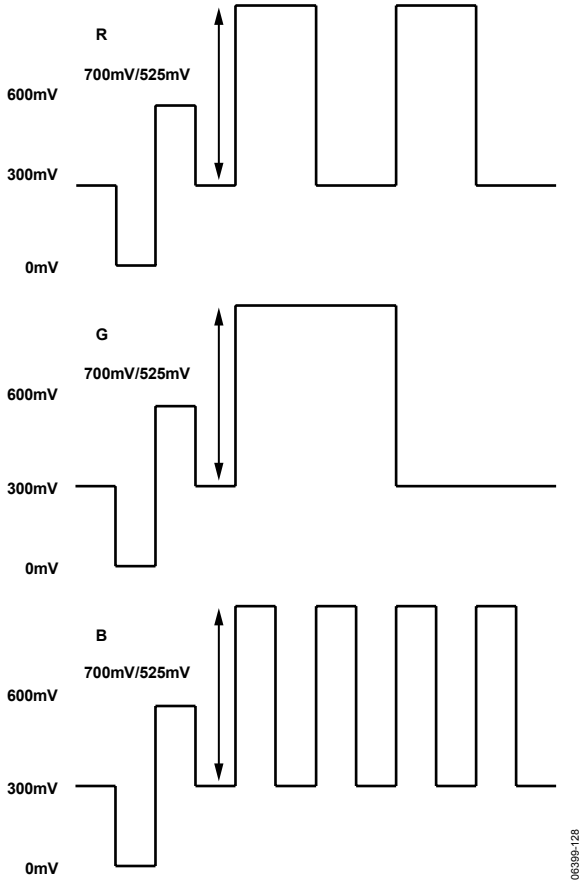


Figure 127. HD RGB Output Levels—RGB Sync Enabled

SD OUTPUT PLOTS

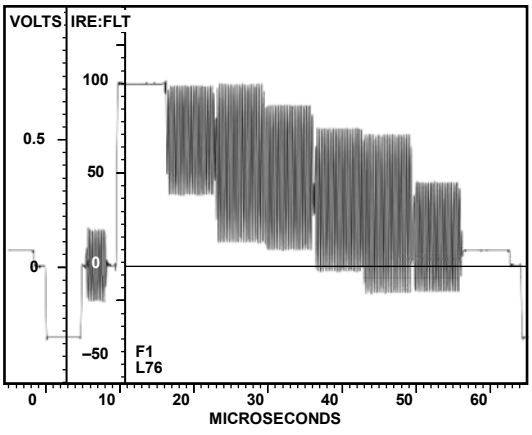


Figure 128. NTSC Color Bars (75%)

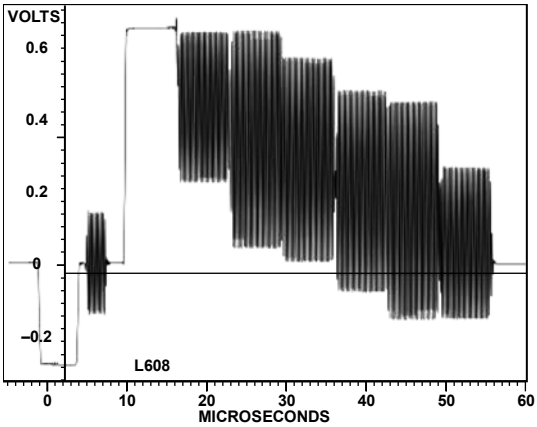


Figure 131. PAL Color Bars (75%)

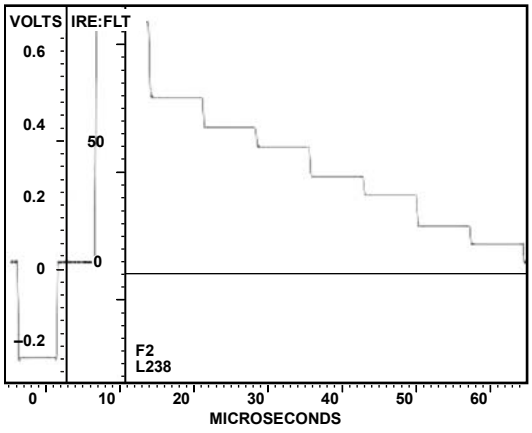


Figure 129. NTSC Luma

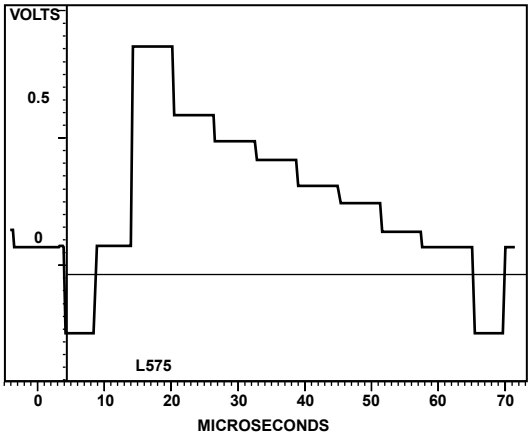


Figure 132. PAL Luma

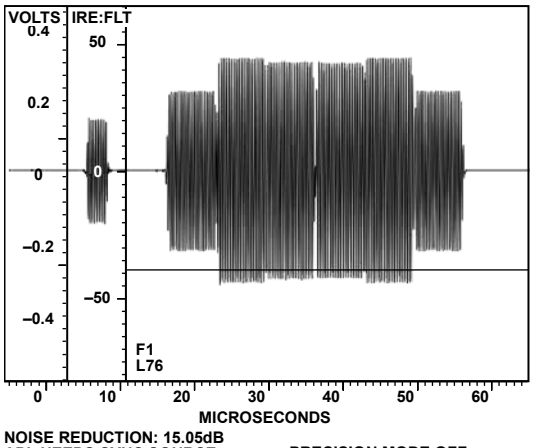


Figure 130. NTSC Chroma

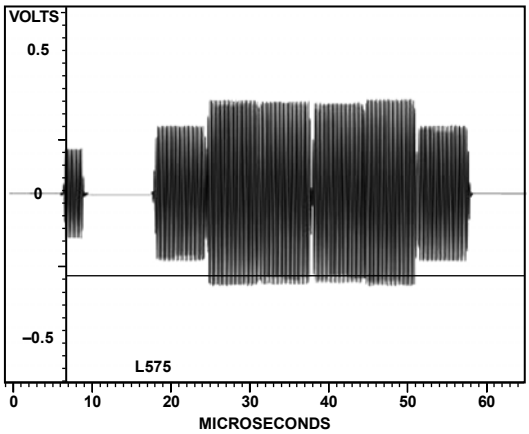


Figure 133. PAL Chroma

APPENDIX 8—VIDEO STANDARDS

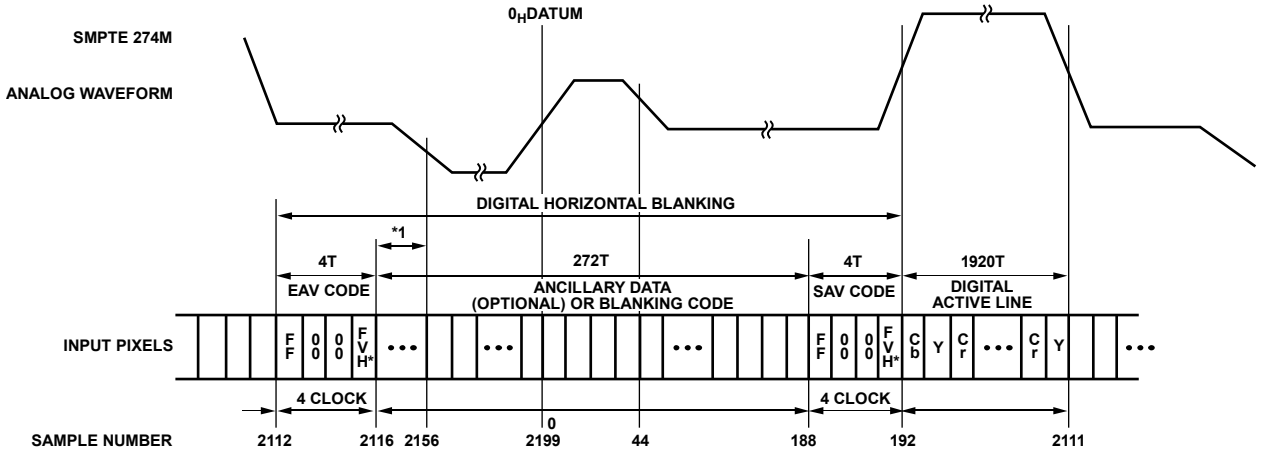


Figure 134. EAV/SAV Input Data Timing Diagram (SMPTE 274M)

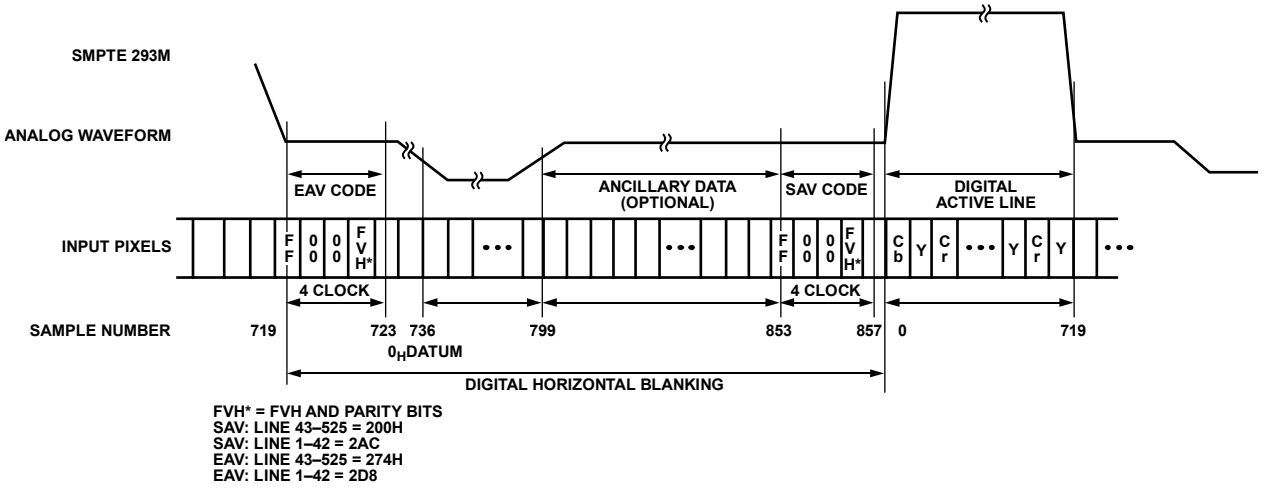


Figure 135. EAV/SAV Input Data Timing Diagram (SMPTE293M)

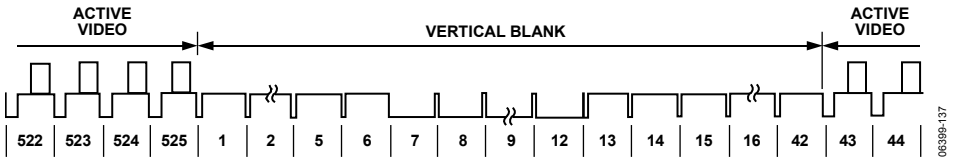


Figure 136. SMPTE 293M (525p)

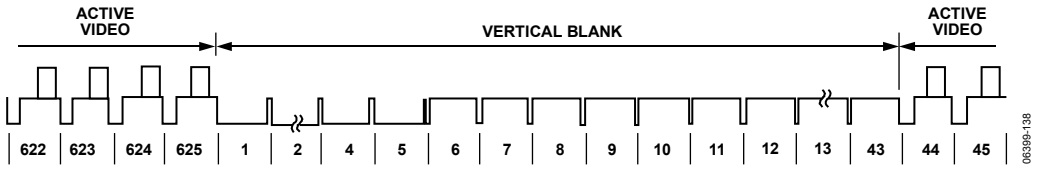


Figure 137. ITU-R BT.1358 (625p)

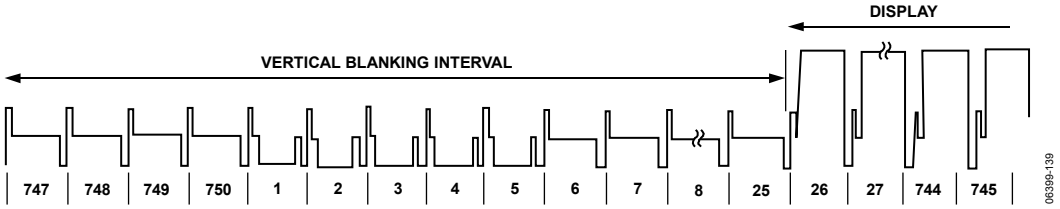


Figure 138. SMPTE 296M (720p)

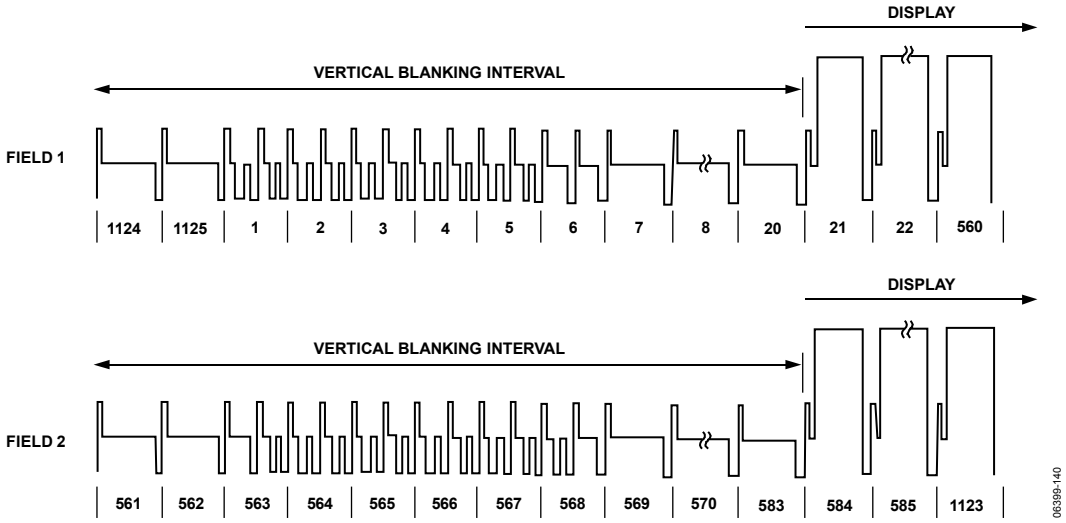
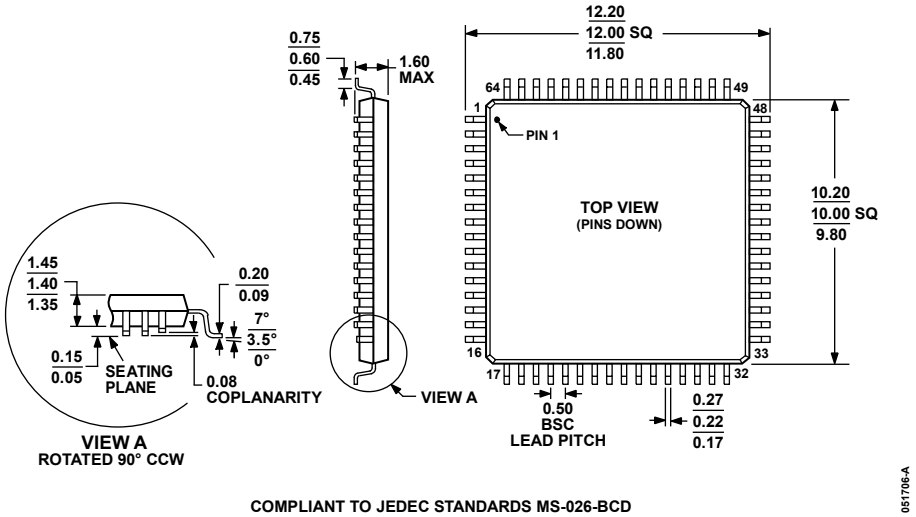


Figure 139. SMPTE 274M (1080i)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BCD

Figure 140. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Macrovision[1] Antitaping	Package Description	Package Option
ADV7342BSTZ[2]	−40°C to +85°C	Yes	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
ADV7343BSTZ[2]	−40°C to +85°C	No	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
EVAL-ADV7342EBZ[2]		Yes	ADV7342 Evaluation Platform	
EVAL-ADV7343EBZ[2]		No	ADV7343 Evaluation Platform	

[1] Macrovision-enabled ICs require the buyer to be an approved licensee (authorized buyer) of ICs that are able to output Macrovision Rev 7.1.L1-compliant video.
[2] Z = Pb-free part.

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

D06399-0-10/06(0)